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ADIABATIC PROCESS TO DESIGN LOW POWER EFFICIENT LOGIC GATES

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Abstract:

The Power Dissipation In Conventional CMOS Circuits Can Be Minimized Through Adiabatic Technique. So, We Are Implementing The Low Power Efficient Logic Using The Microwind Software. It Deals With How This Process Is Implementing The Reversible Logic And Making Use Of Stored Power. In Earlier Circuits Power Dissipated Is Very High Due To Charge Transfer Between PMOS And NMOS Which Results In Much Delay And Larger Dissipation Of Heat. In Case Of Adiabatic Logic We Have Several Methods Such As Efficient Charge Recovery Logic (ECRL), Positive Feedback Adiabatic Logic (PFAL) And Many More Such As Enhanced Ecrl, Quasi Adiabatic Logic (QAL). All These Will Be Implementing The Circuit In Advanced Way Of Utilizing The Complete Charge Which Make Them More Efficient. In Our Project We Are Dealing With Mainly Two Of The Techniques: ECRL And PFAL With Basic Gates Of Inverter, Nand And Nor To Compare The Parameter.So, In The Micro Wind Software We Design The VLSI Layouts Of The Logic Gates And Compare The Power Dissipated By Them Changing Various Parameters And Comparing The Conventional Logic Family With The Advanced Version Of Designs. This Will Result In Improving The Efficiency Of The Several Circuits As The Basic Gates Power Dissipation Is Reduced. And Even As The Heat Is Been Reduced There Isn't Much Need Of Cooling Equipments To Reduce The Temperatures Of The Processors And Controllers.Hence, It Has Got Several Applications In The Developing VLSI Field And As Well As Micro Level Integration Of The Chips. This Could Be Further Being Extended To Design Even Other Gates Using The Same Logic And Improve Their Efficiency.

Keywords: CMOS Circuits, ECRL, QAL, PFAL

1 Introduction:

The term "adiabatic" describes the thermodynamic processes in which no energy exchange is with the environment, and therefore no dissipated energy loss. But in VLSI, the electric charge transfer between nodes of a circuit is considered as the process and various techniques can be applied to minimize the energy loss during charge transfer event. Fully adiabatic operation of a circuit is an ideal condition for its operation. It may be only achieved with very slow switching speed. In practical cases, energy dissipation with a charge transfer event is composed of an adiabatic component and a non-adiabatic component.

In conventional CMOS logic circuits, from 0 V to 5 V transition of the output node, the total output energy drawn from power supply and stored in capacitive network. Adiabatic logic circuits reduce the energy dissipation during switching process, and utilize this energy by recycling from the load capacitance. For recycling, the adiabatic circuits use the constant current source power supply and for reduce dissipation it uses the trapezoidal or sinusoidal power supply voltage. The equivalent circuit used to model the conventional CMOS circuits during charging process of the output load capacitance.So, power dissipated in these conventional circuits and consumed is high and even leads to lot of delay. This is one of the major problems in these circuits which is to be reduced by utilizing the charge properly without wasting it during the transmission across each other transistors.

3 CMOS CIRCUITS:

The types of logic circuits are

1. CMOS INVERTER
2. CMOS NAND
3. CMOS NOR

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1. CMOS INVERTER:

The most important CMOS gate is the CMOS inverter. It consists of only two transistors, a pair of one N-type and one P-type transistor. Fig.1.1 shows the basic circuit of CMOS Inverter. Voltage levels are at logical '1' corresponding to electrical level VCC, a logical '0' (corresponding to 0V or GND).

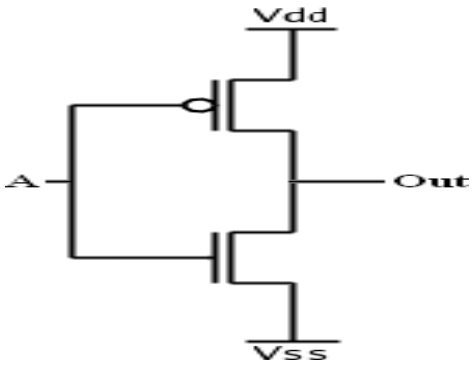

Figure:1 CMOS Inverter circuit

So, whenever the input is 'HIGH' its corresponding output is 'LOW' and vice- versa. The above circuit is made up of PMOS transistor (which are pull-up) and below.are the NMOS transistor (which are pull-down). These two together combine to make the circuit function as inverter.

2. CMOS NAND:

A NAND gate (Negated AND or NOT AND) is a logic gate which produces an output that is false only if all its inputs are true. A LOW (0) output results only if both the inputs to the gate are HIGH (1); if one or both inputs are LOW (0), a HIGH (1) output results. The NAND gate is significant because any Boolean function can be implemented by using a combination of NAND gates. This property is called functional completeness.

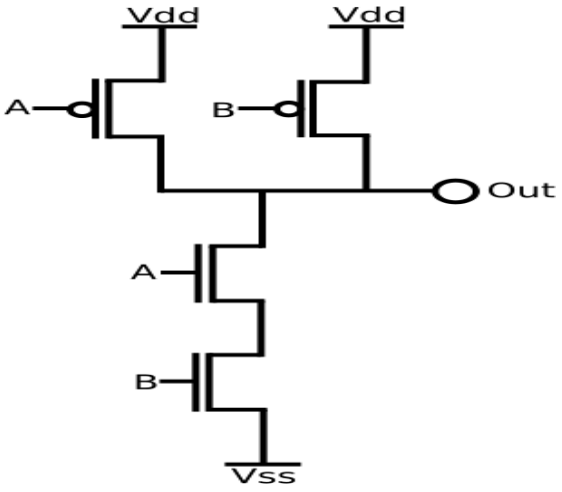

Figure 2: CMOS NAND circuit

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3 CMOS NOR:

The NOR gate is a digital logic gate that implements logical NOR - it behaves according to the truth table to the right. A HIGH output (1) results if both the inputs to the gate are LOW (0); if one or both input is HIGH (1), a LOW output (0) results. NOR is the result of the negation of the OR operator. It can also be seen as an AND gate with all the inputs inverted. NOR is a functionally complete operation— combinations of NOR gates can be combined to generate any other logical function. By contrast, the OR operator is monotonic as it can only change LOW to HIGH but not vice versa.

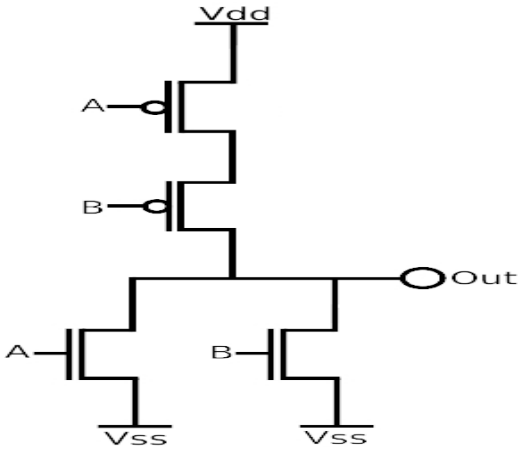

Figure 3: CMOS NOR circuit

4 Microwind:

It is integrated software encompassing IC designs from concept to completion, enabling us to design the chips beyond our imagination. It integrates mixed-signal implementation with digital implementation, circuit simulation, transistor-level extraction and verification.It unifies schematic entry, pattern based simulator, SPICE extraction of schematic, Verilog extractor, layout compilation, on layout mix-signal circuit simulation, cross sectional & 3D viewer, netlist extraction, BSIM4 tutorial on MOS devices and sign- off correlation to deliver unmatched design performance and designer productivity.The basic Microwind layout design platform is going to be as follows as shown in the figure below

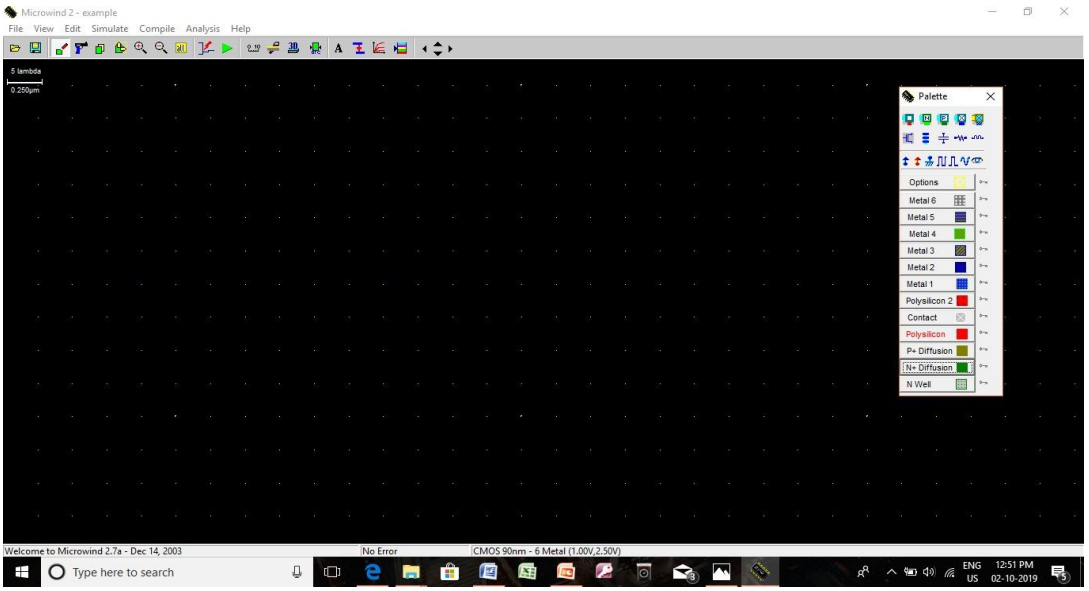

Figure 4:Microwind layou

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5 An Adiabatic System:

Two main parts of an adiabatic system are (i) Digital core design made up of adiabatic gates and the power-clock signal generator. We have used two adiabatic families in this paper. The most important aspect of the adiabatic system is clock- signal generation; High saving factors can be achieved by an optimal generation of four-phase power-clock.Two adiabatic logic families are discussed in the current paper, one is Positive Feedback Adiabatic Logic (PFAL) and the other is the Efficient Charge Recovery Logic (ECRL). Both operate in the same four-phase power-clock supply. PFAL is designed by the cross coupling of two inverters, which is the latch element. They store the output state when the input signal gradually decreases. A cross coupled PMOS pair is used in case of ECRL based on Cathode Voltage Switch Logic (CVSL). PFAL and ECRL use logic block constructed from NMOS. Logic blocks are connected from the power clock Φ to the output nodes for PFAL and from the output to Ground for ECRL.

6 Efficient Charge Recovery Logic:

Efficient Charge Recovery Logic (ECRL) is proposed as a candidate for low- energy adiabatic logic circuit. Power comparison with other logic circuits is performed on an inverter chain. It adopts a new method that performs pre-charge and evaluation simultaneously. ECRL eliminates the pre-charge diode and dissipates less energy than other adiabatic circuits. An ECRL inverter chain and a pipelined Carry Look Ahead Adder (CLA) are constructed to show the effectiveness of this approach.

6.1 ECRL INVERTER:

In ECRL inverter, two inverter are cross- coupled to each other and one inverter's input is other's output and vice versa. The ECRL inverter works same as that of basic operation of ECRL.

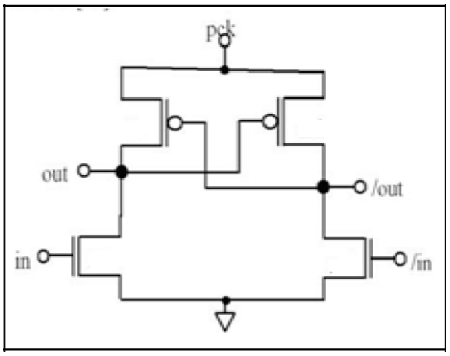

Figure 5: ECRL Inverter Circuit

6.2 ECRL NAND CIRCUIT:

The figure shown above is ECRL NAND. It functions same as that of CMOS NAND circuit

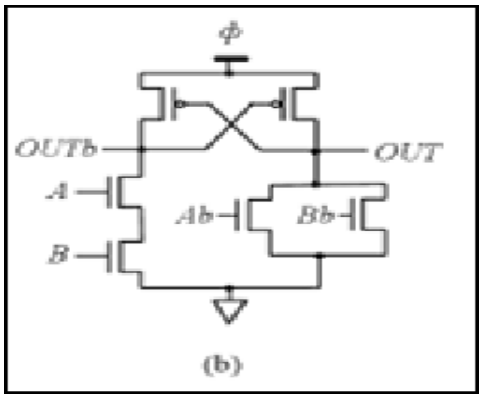

Figure 6: ECRL NAND Circuit

When both inputs are low then output is high and when both the inputs are high then output is low. When one input is high and the other is low then the output is one and vice versa. Thus ECRL consumes less power

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compared to CMOS NAND gate. Hence we prefer ECRL nand gate in place of CMOS NAND gate.
ECRL NOR CIRCUIT

The fig. shows ECRL NOR circuit functions same as that of CMOS NOR circuit.

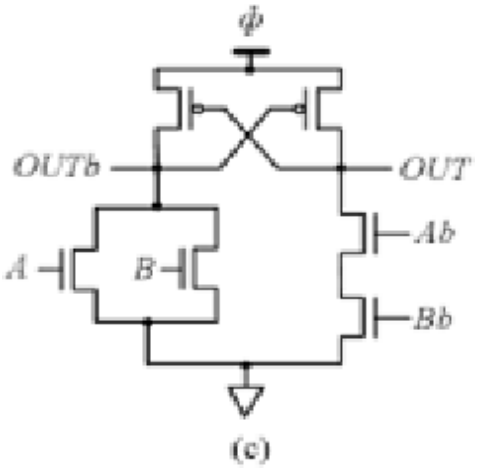

Figure 7: ECRL NOR Circuit

According to the waveform when both the inputs are high then the output is low. After that when both the inputs are low then the output is high. If one input is high and the other is low then the output is zero or vice versa.

6.3 POSITIVE FEEDBACK ADIABATIC LOGIC:

The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) has been used, since it shows the lowest energy consumption if compared to other similar families, and a good robustness against technological parameter variations. It is a dual-rail circuit with partial energy recovery . The general schematic of the PFAL gate is shown in Figure 1. The core of all the PFAL gates is an adiabatic amplifier, a latch made by the two PMOS M1-M2 and two NMOS M3-M4, that avoids a logic level degradation on the output nodes out and /out. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs.

6.4 PFAL INVERTER:

The inverter (NOT circuit) performs the operation called inversion or complementation. The NOT operation changes one logic level to the opposite logical level. When the input is Low, the output is high. When the input is high, the output is low. The inverter changes one logic level to the opposite level. In terms of bits, it changes a 1 to a 0 and 0 to 1. When a High level is applied to an inverter input, a low level will appear on its output. When a low level is applied to its input, a High will appear on its output. PFAL based NOT gate is shown in Figure.

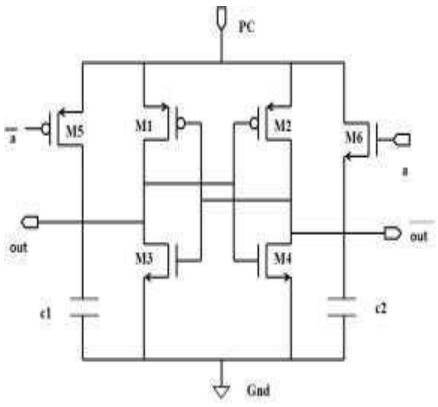

Figure 8: NOT gate using PFAL

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6.5 PFAL NAND CIRCUIT:

NAND gate is an electronic circuit which has two or more inputs but only one output. The NAND gate is the natural implementation for the simplest and fastest electronic circuits. The output is HIGH if at least one of its inputs is LOW. The output is LOW only when all the inputs are HIGH. The term NAND is a contraction of NOTAND. The NAND gate is a combination of an AND gate followed by NOT gate. For 2 input NAND gate, two NMOS transistors connected in series is taken as pull down network and two PMOS transistors connected in series is taken as pull up network.
PFAL based NAND gate structure is shown in Figure 3. This circuit works similar to CMOS technology based circuit and also reduces power by recycling the energy instead of discharging it to ground.

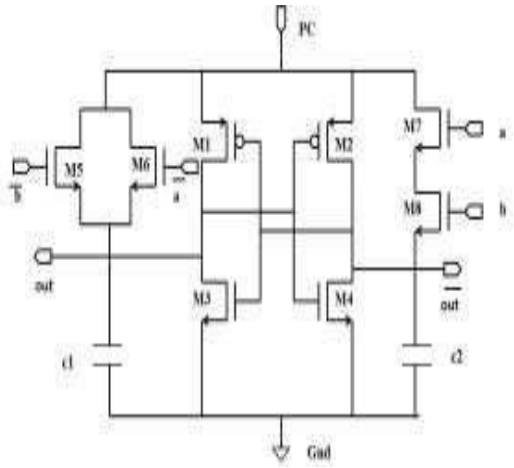

Figure 9 :NAND gate using PFAL

6.6 PFAL NOR CIRCUIT:

The NOR gate, like the NAND gate, NOR gate is also useful logical element because it can also be used as a universal gate. NOR gate can be used in combination to perform the AND, OR and Inverter operations.
NOR Gate is the combination of NOT gate at the output of OR gate, hence NOR gate is type of NOT-OR gate. NOR gate has two or more input and only one output. The Output of NOR gate is high when all inputs are low otherwise the output is low.PFAL based NOT gate is shown in Figure which has similar operation to CMOS technology with less power consumption.

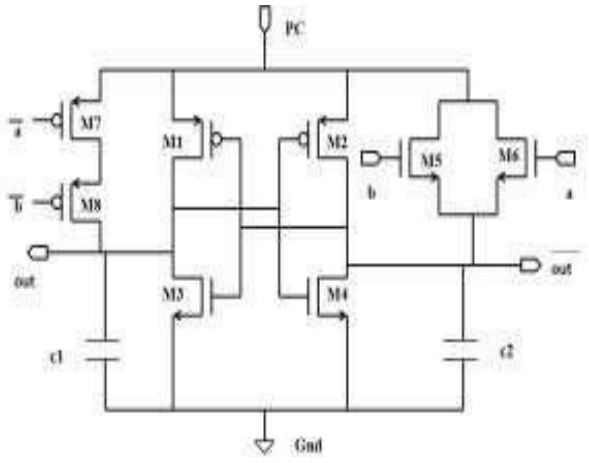

Figure 10: NOR gate using PFAL

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7 Results:

Layouts Of Simulations In Microwind:

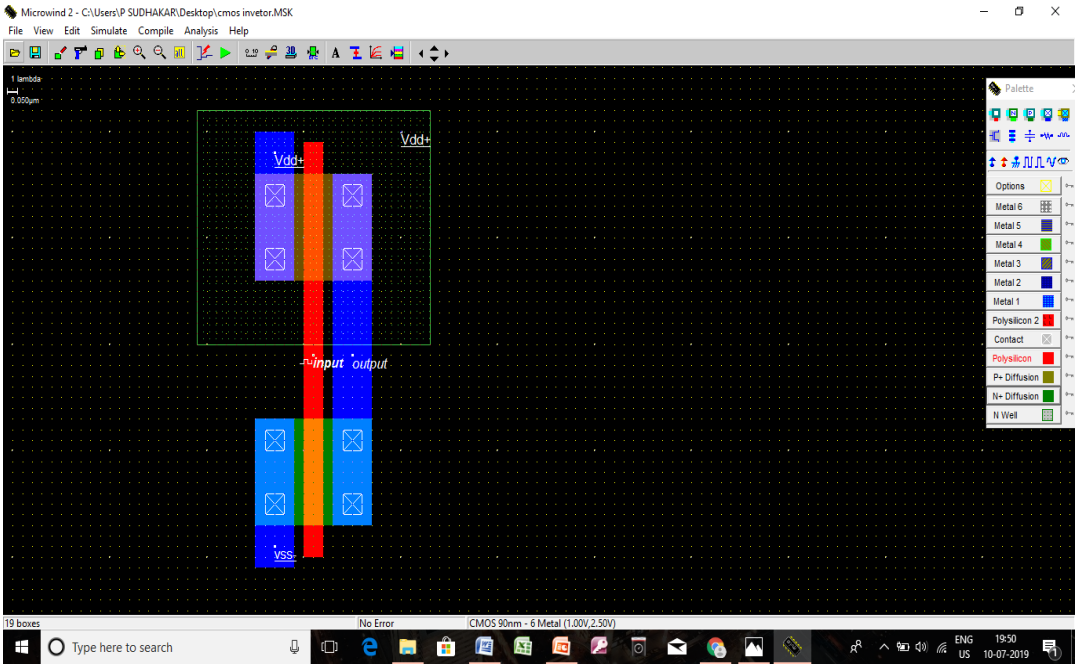

Figure 11: Layout of CMOS inverter

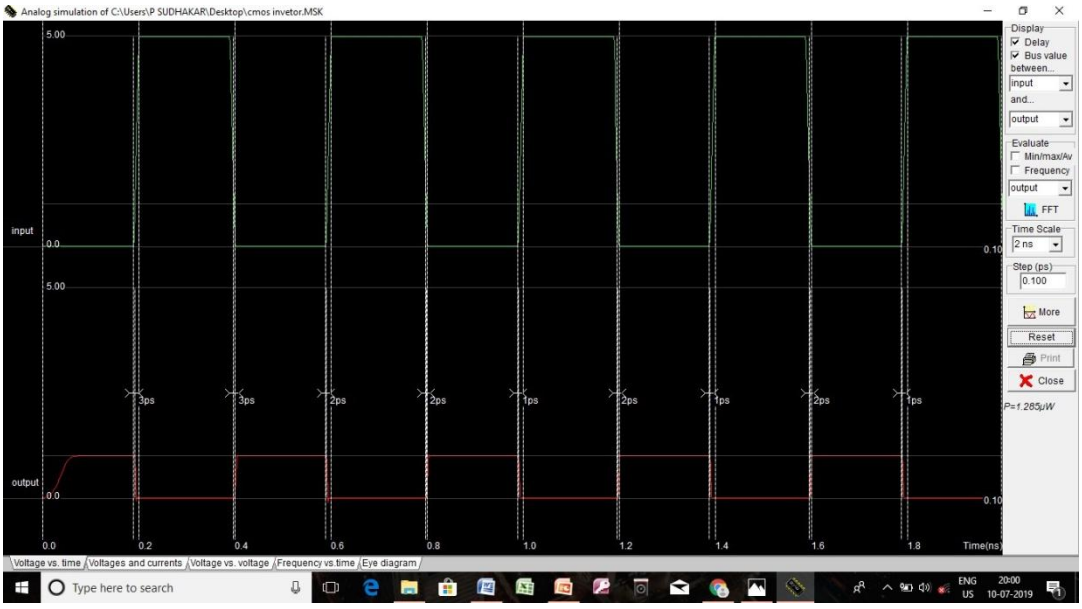

Figure 12: Simulation of CMOS inverter

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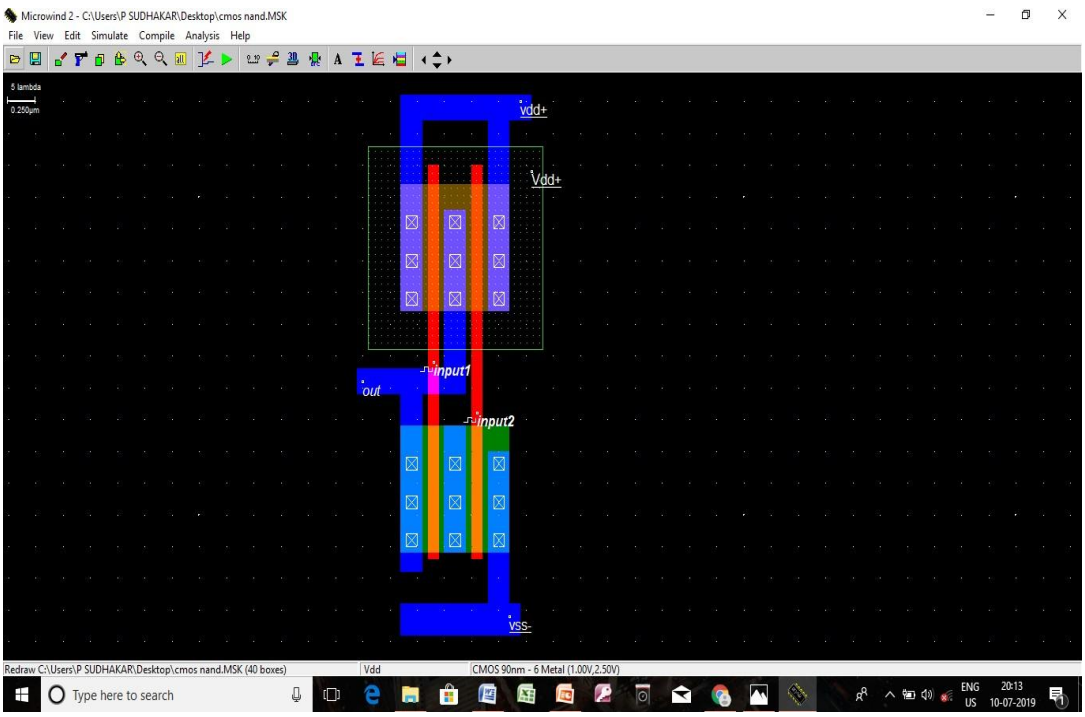

Figure 13: Layout of CMOS NAND

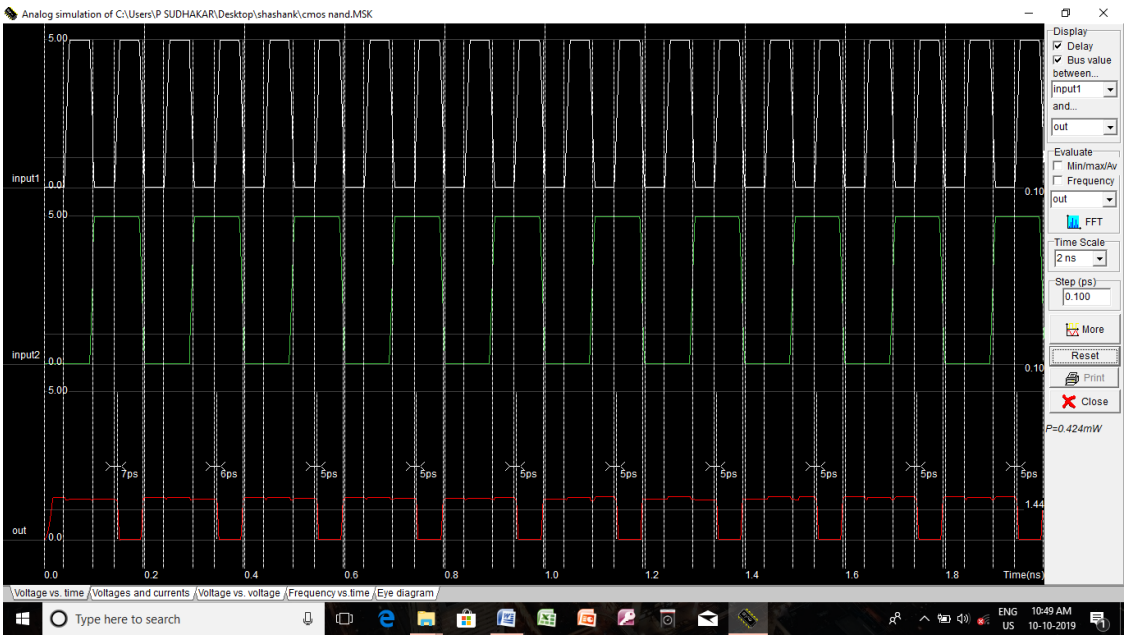

Figure 14: Simulation of CMOS NAND

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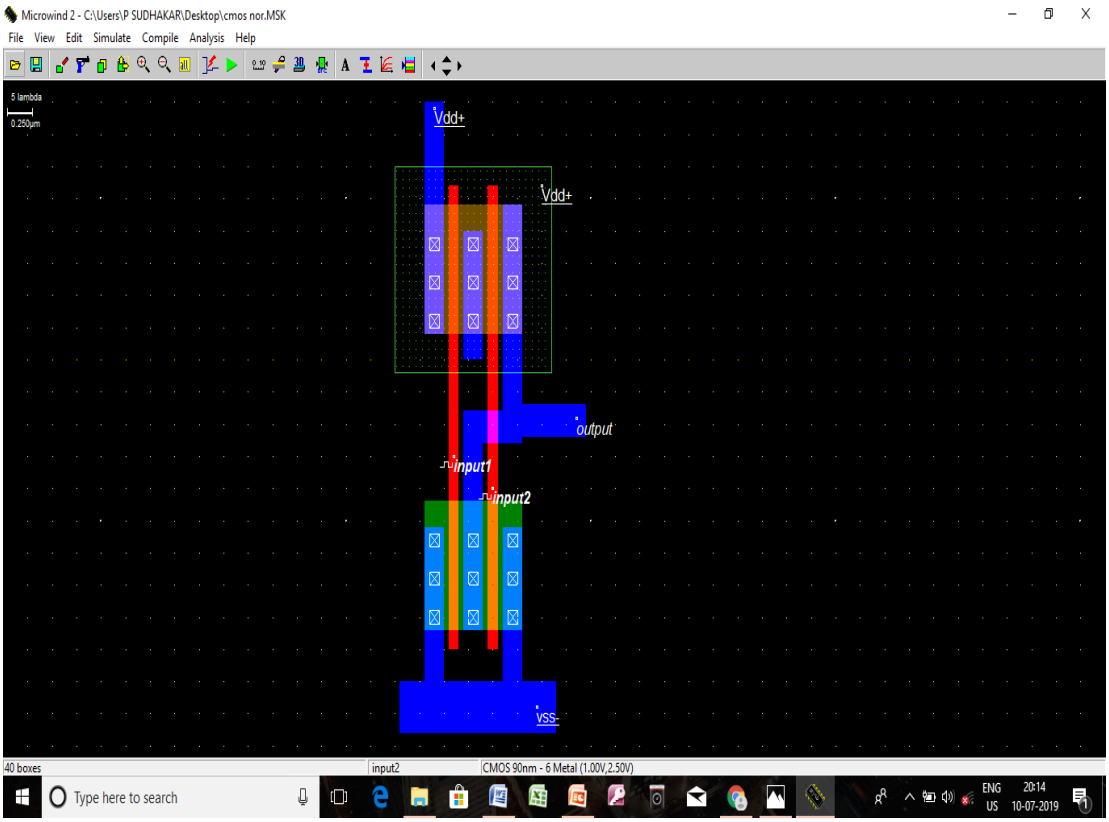

Figure 15: Layout of CMOS NOR

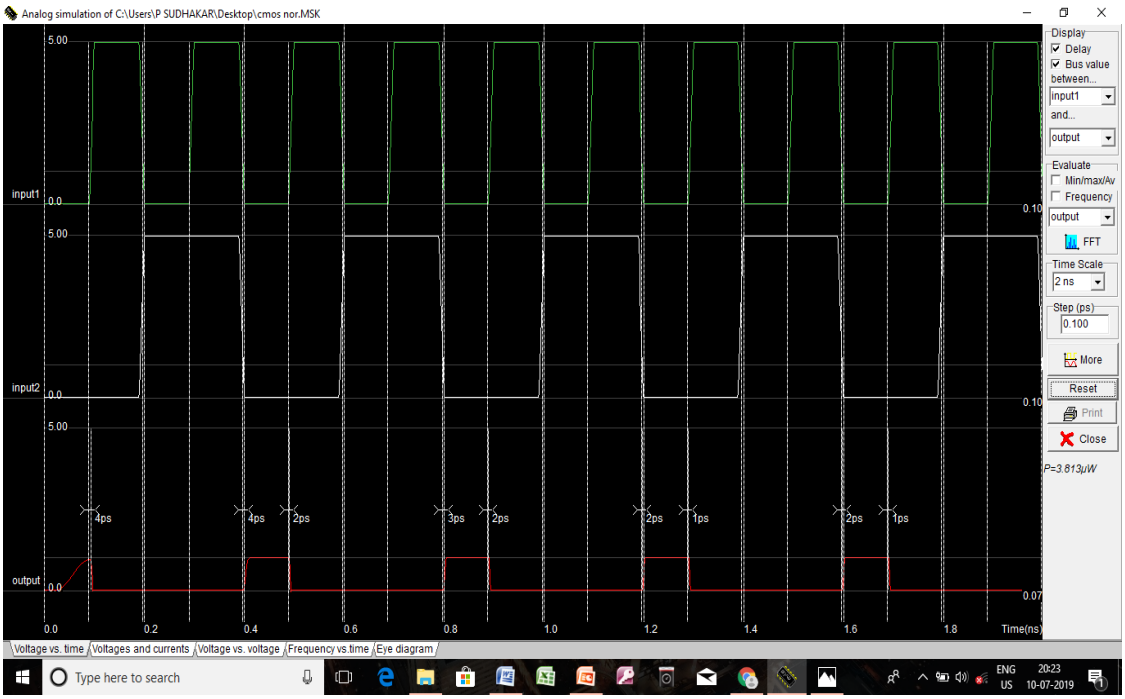

Figure 16 : Simulation of CMOS NOR

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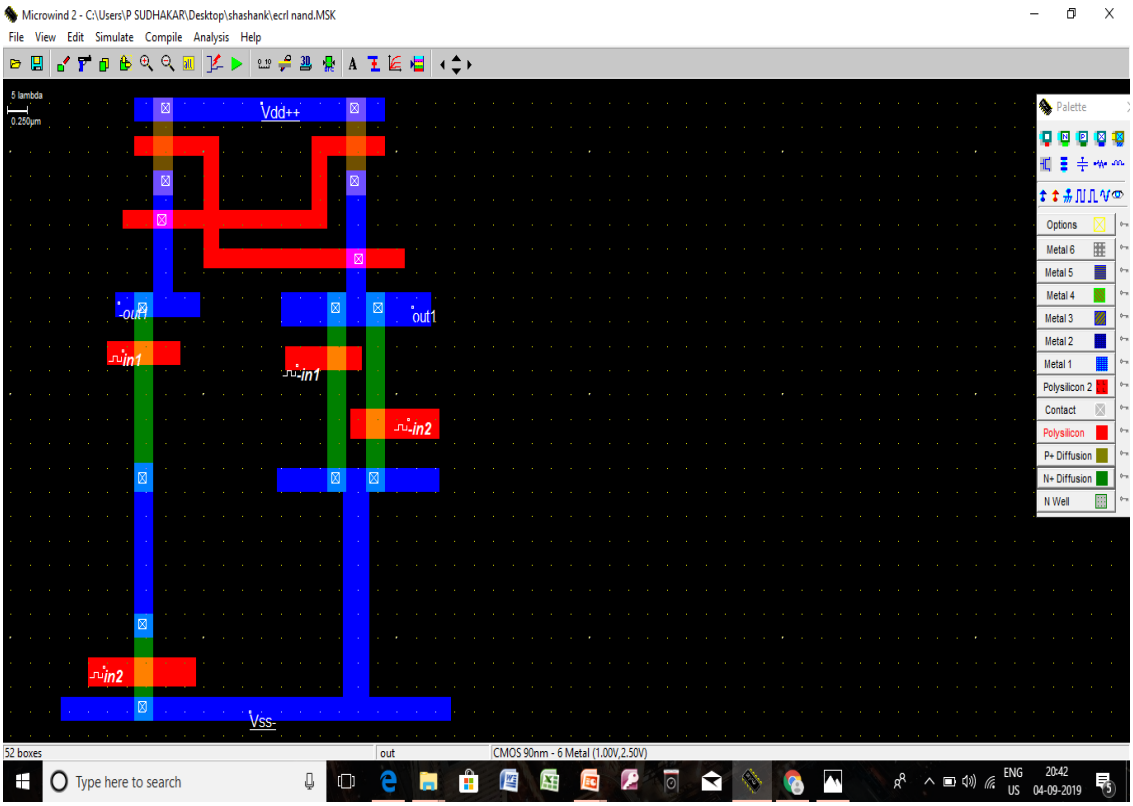

Figure 17 : Layout of ECRL NAND

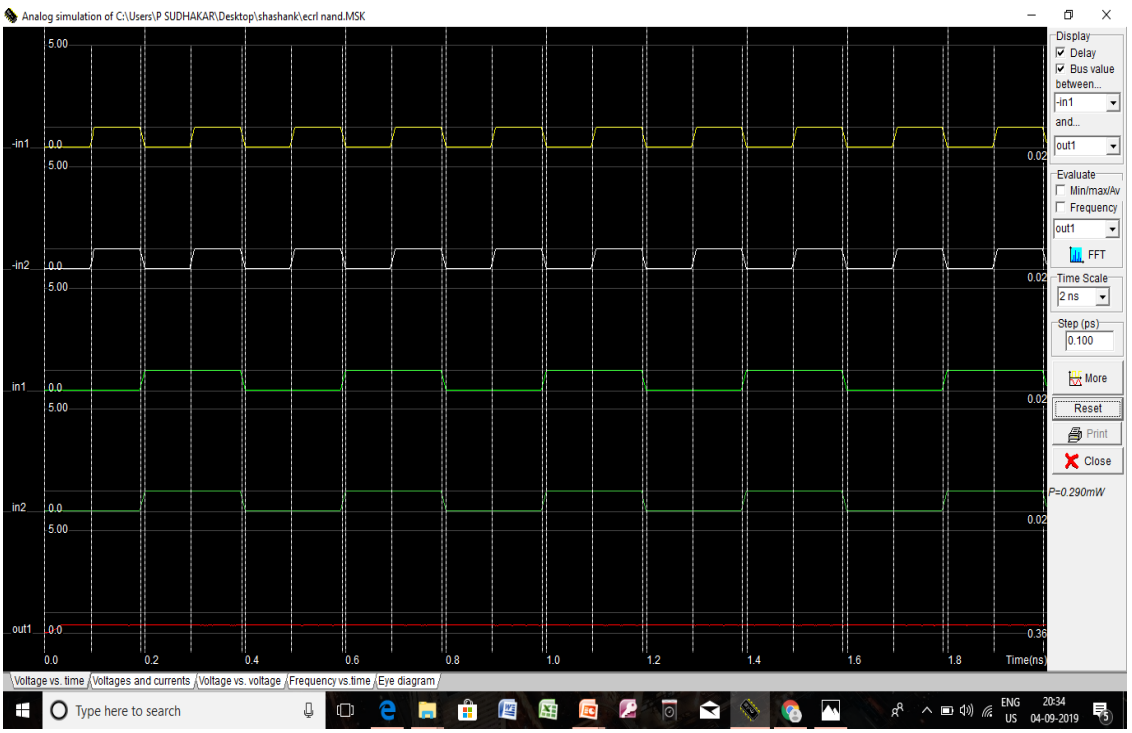

Figure 18: Simulation of ECRL NAND

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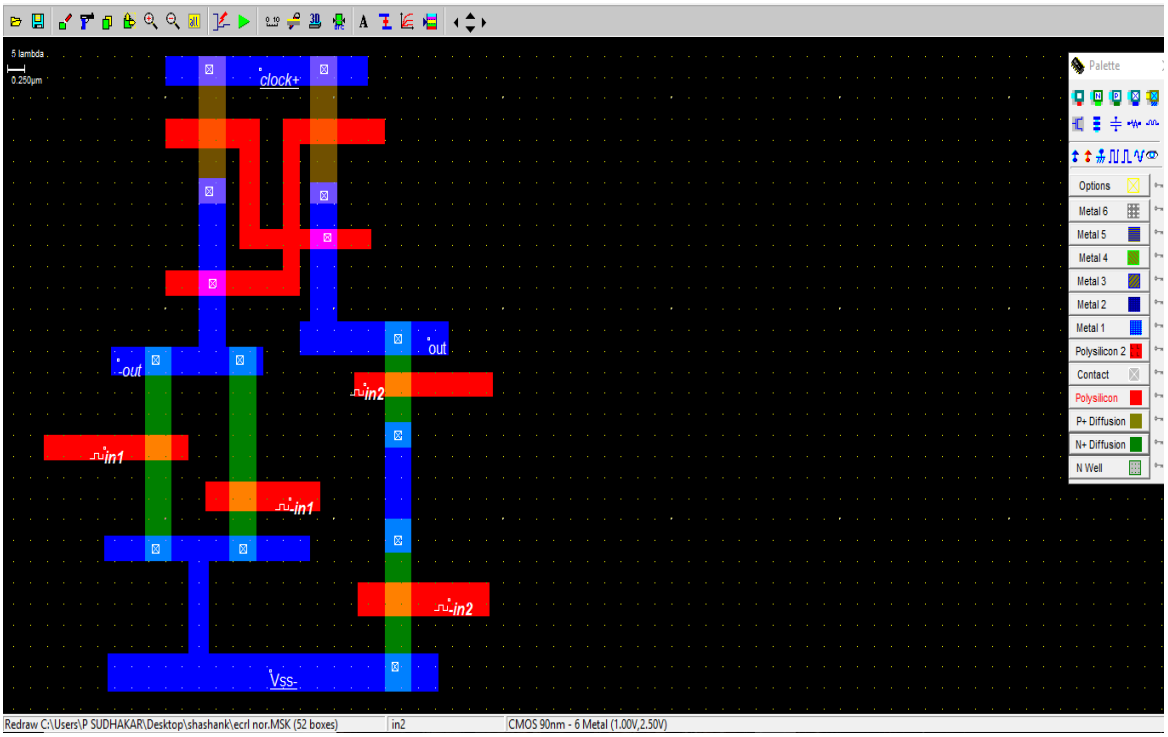

Figure 19: Layout of ECRL NOR

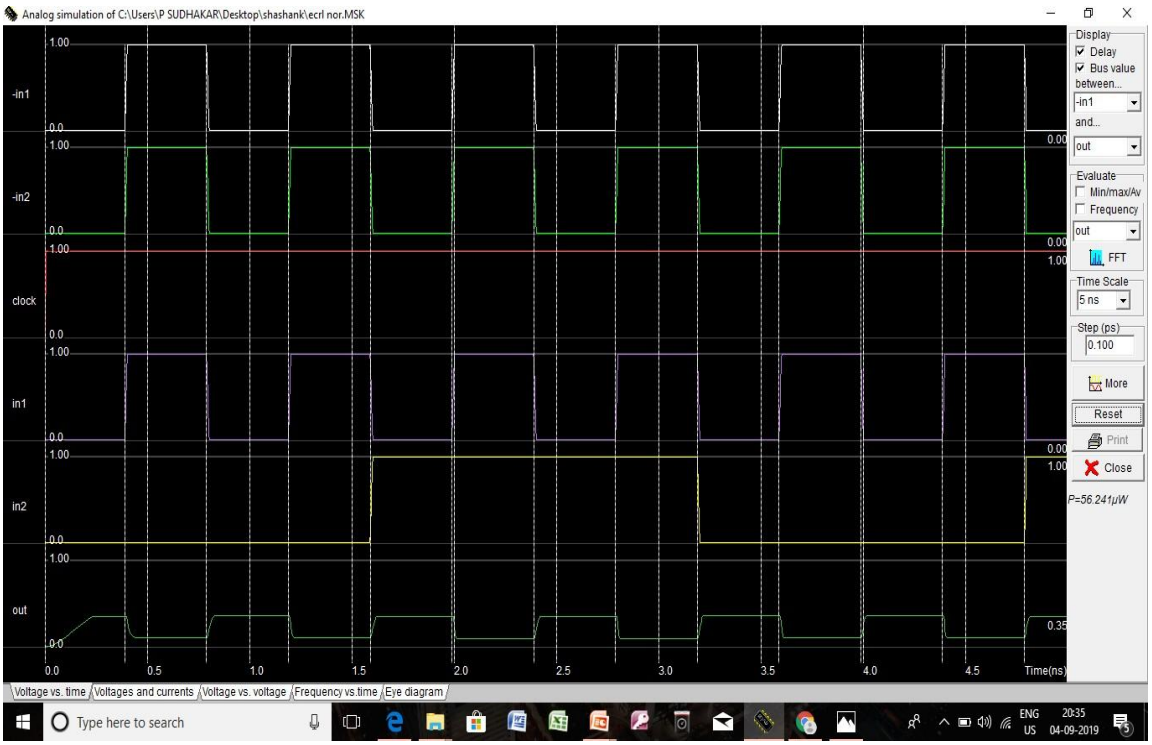

Figure 20: Simulation of ECRL NOR

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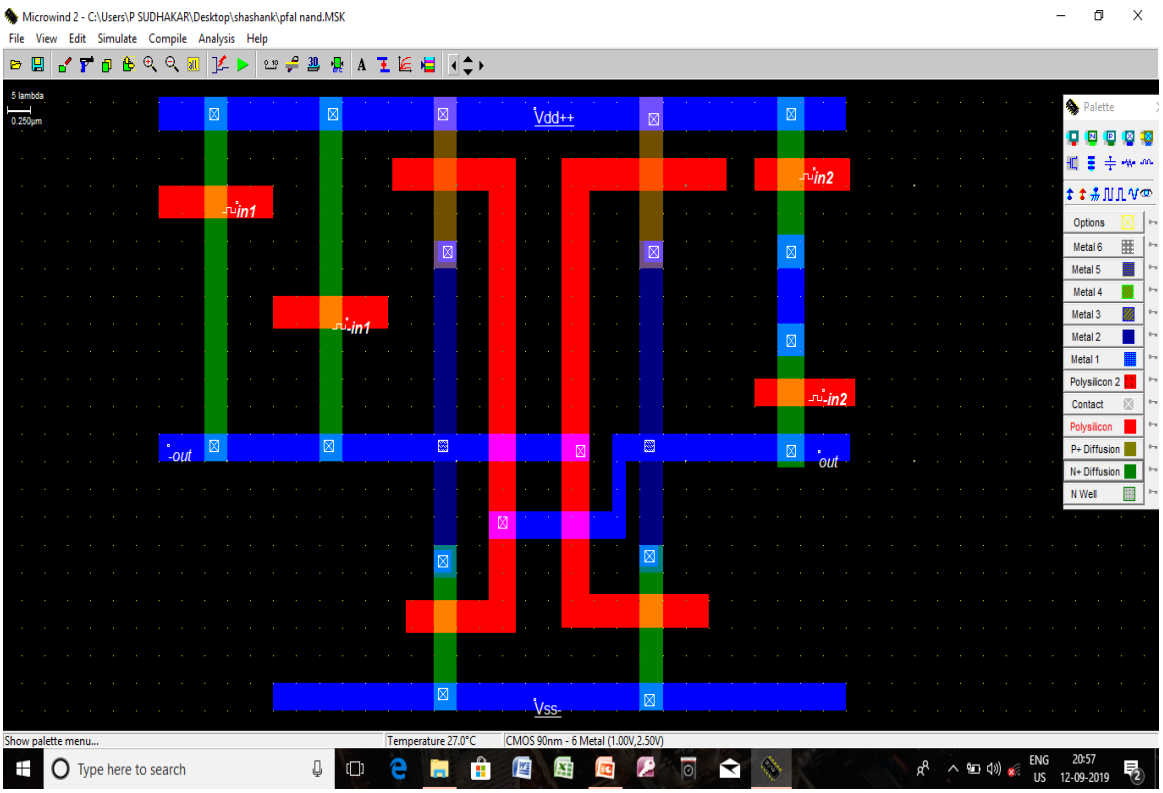

Figure 21: Layout of PFAL NAND

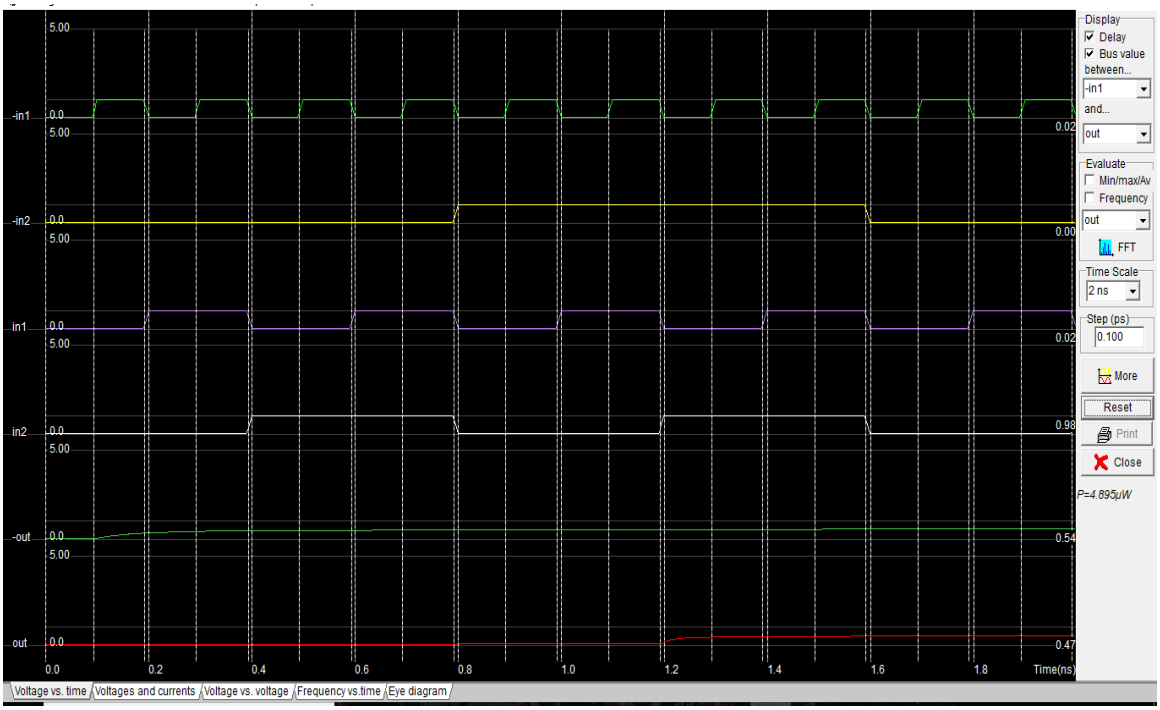

Figure 22: Simulation of PFAL NAND

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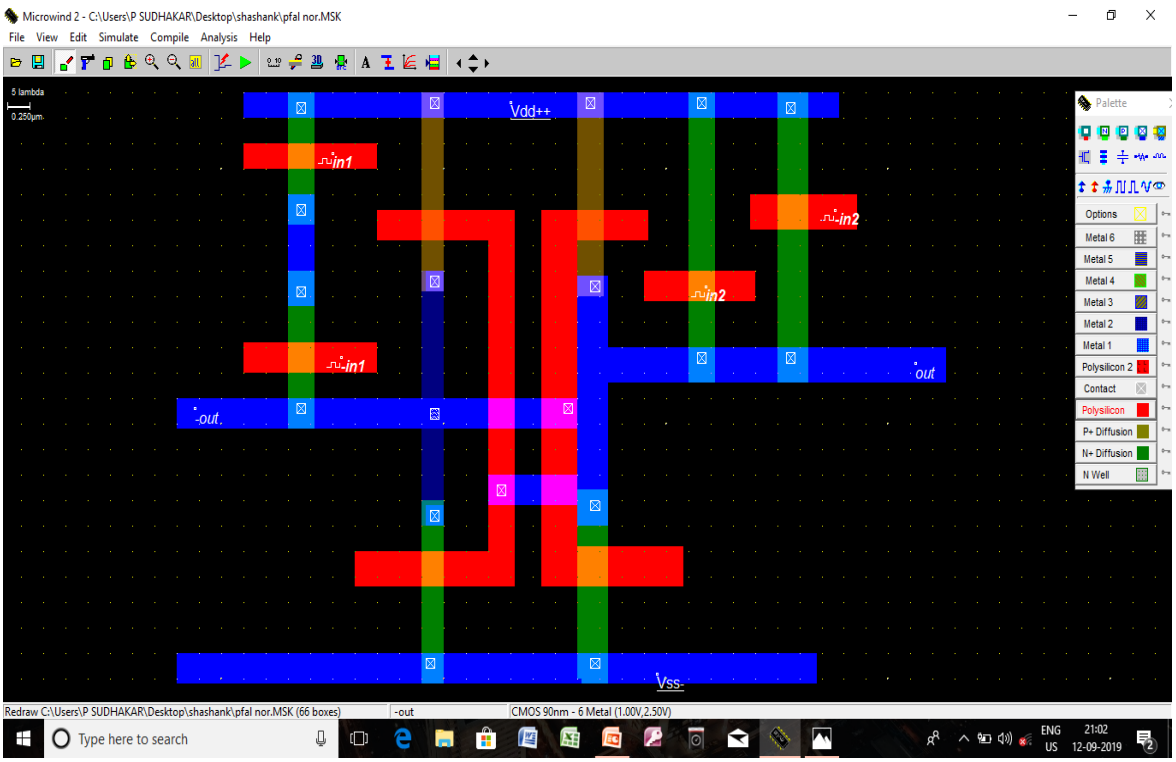

Figure 23: Layout of PFAL NOR

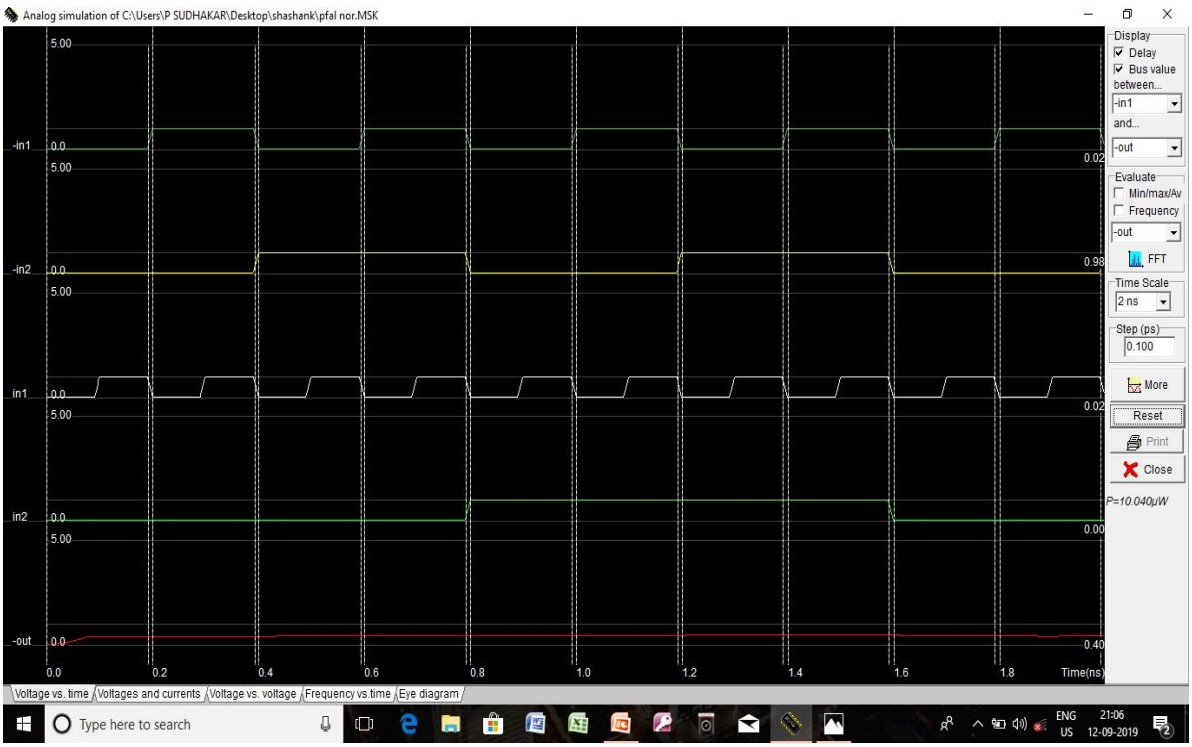

Figure 24 :Simulation of PFAL NOR

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S.NO		CMOS		ECRL		PFAL	
		SV	PD	SV	PD	SV	PD
1	Inverter	1V	1.28µW	-	-	-	-
2	NOR	3.3V	0.10mW	3.3V	97.81µW	3.3V	9.95µW
3	NAND	3.3V	0.42mW	3.3V	0.27mW	3.3V	4.93µW

Table 1: observed values of desired parameters

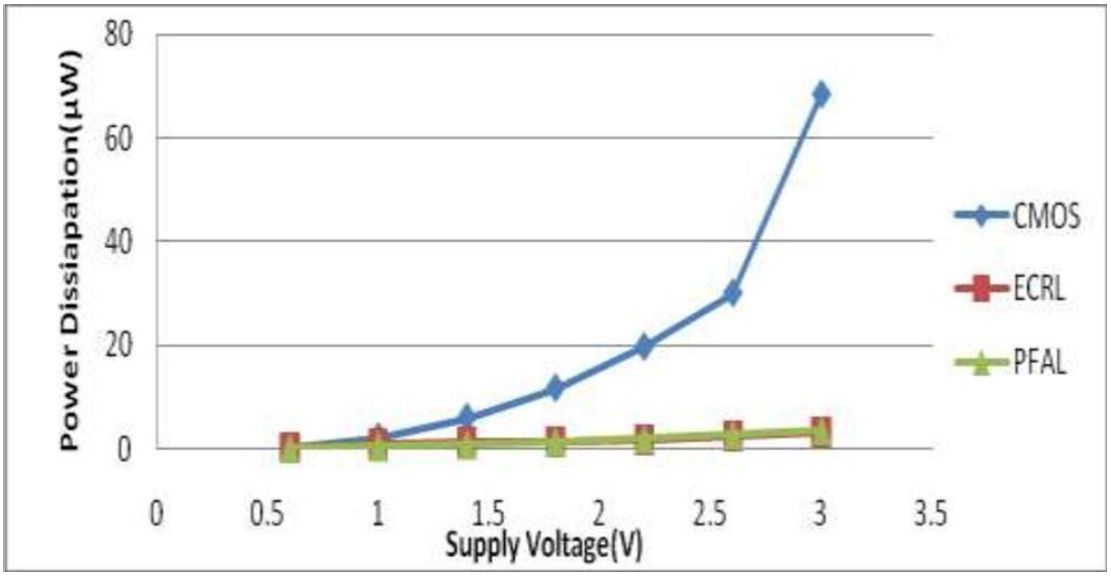

Figure 26: Comparison between various logic families

8 Conclusion & Future scope:

As seen in the above cases complementary mos logics have power consumed around 0.4 milliwatt(for NAND) and 96.47 microwatt(for NOR). This is been reduced in adiabatic logics to 0.290 milliwatt and 76.34 microwatt. And further been reduced in positive feedback adiabatic logic to 10.48 microwatt and 4.86 microwatt and comparison characteristics can be drawn for all the three

We use this basic design structure to build higher complex circuits such as comparators or multipliers. That is we can design higher end multiple number of adders, subtractors, encoders and decoders at a time.
We can also design single circuit to perform all the operations with low power dissipation, such as a magnitude comparator can be designed from these basic gates which will consume less power than conventional one in market.
Even technology these days are working on creating larger number of gates on single chip of controller, but face typical power issues. So, this techniques can be used to overcome that drawback

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