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DESIGN AND SIMULATION OF HETEROGENEOUS ADDER USING XILINX VIVADO

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Abstract **–**Adders are the logic circuits designed to perform high speed Arithmetic operations in the Arithmetic Logic Unit used in the processors. The basic Adders are Half Adder and Full adder. Different types of adders are Ripple Carry Adder(RCA), Carry Look ahead Adder(CLA), Carry Skip Adder(CSKA), Carry Select Adder(CSLA). In this paper, Heterogeneous adder architecture is designed with the help of different Homogeneous adders and Heterogeneous adders are compared with the Homogeneous adders in terms of Area, Delay and Power. This architecture is based on a VHDL and compares their performance with Xilinx VIVADO software tool.

Keywords- Adders, Ripple Carry Adder, Carry Look ahead Adder, Simulation, VHDL, etc.

I . INTRODUCTION

Arithmetic operations play an important role in various digital systems. Adders are the key components in general purpose Microprocessors and Digital signal Processors. Adders are used to perform the Addition of numbers, Multiplication ,Subtraction and Division operations. They require low efficient power and area designed technique to increase the performance of the circuit. Therefore, the area efficient design makes the chip size smaller ,reduces the cost. The different adders are Ripple Carry Adder, Carry Look ahead Adder, Carry Select Adder, Carry Skip Adder.

Here Heterogeneous adder means concatenation of different homogeneous adders and Homogeneous adder is the combination of the same type of adders. The designed adder is compared with each other in terms of area and power along with the simulation result and implementation using Xilinx VIVADO.

II. RELATED WORK

A. Ripple Carry Adder:

Ripple carry adder can be designed by cascading full adder in series i.e., carry from previous full adder is connected as input carry for the next stage. Full adder is a basic building block of Ripple carry adder. Therefore, to design a n-bit parallel adder, it requires n full adders. The block diagram of Ripple carry adder is as shown below

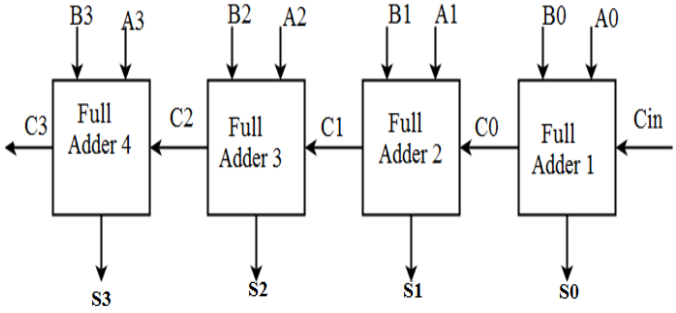

Fig.1: 4-Bit Ripple Carry Adder

Example: A=1010 ; B=0101 ;Cin =0 are the inputs of the adder than the output is S=1111 with a carry '0'.

The major limitation of ripple carry adder is that as the bit length goes on increase, delay also increases.Since each full adder must wait for the carry bit from the previous full adder. So Ripple carry adder is relatively slow.

B. Carry Look Ahead Adder:

Carry Look ahead adder is also known as the Fastest Adder. It improves the speed by reducing the amount of time required to determine the carry bits. The block diagram of the Carry Look aheadAdder is as shown below

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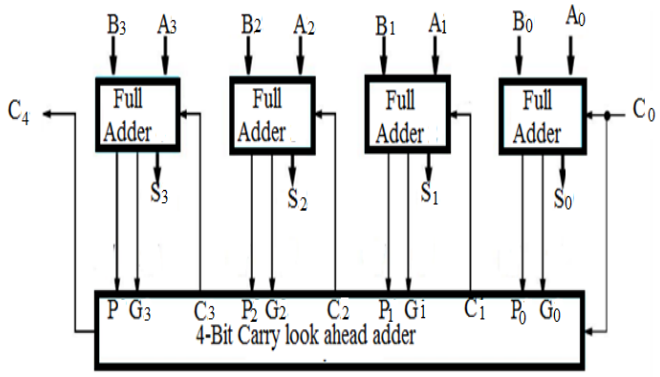

Fig.2: 4-Bit Carry Look Ahead Adder

The carry look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits. The working of this adder can be understood by manipulating Boolean expressions dealing with full adder and it is given by

Carry propagate(Pi) = A xor B

Carry Generate(Gi) = A and B

Both propagate and generate signals depend only on input signals, the new expressions for output sum and carry are

Sum(Si)= Pi xor Ci ;

Carryout(Ci+1)=Gi+ Pi Ci

The limitation in the Carry look ahead adder is if the bit length goes on increasing the circuit complexity is also increased.

C. Carry Select Adder:

The Carry select adder consists of two ripple carry adders and a multiplexer. It consists of an independent generation of sum and carry is Cin=1 and Cin=0 are executed parallel. Depending upon the Cin the external multipliers select the carry to the next stage. Further based on the carry input the sum will be selected hence the delay is reduced. The block diagram of the Carry select adder is as shown below

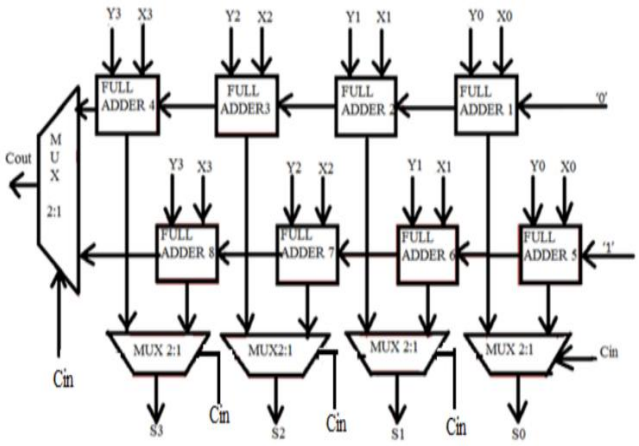

Fig.3: 4-Bit Carry Select Adder

D. Carry Skip Adder:

Carry skip adder is also known as carry Bypass adder and that improves on the delay of Ripple carry adder. The improvement of the worst delay is achieved by using several carry skip adders to form a block skip adder.

The skip logic consists of a m-input AND-gate and one multiplexer. As the propagate signals are compared in parallel and are early available, the critical path for the skip logic in carry skip adder consists only of the delay imposed by the multiplexer. The block diagram of the carry skip adder is as shown below

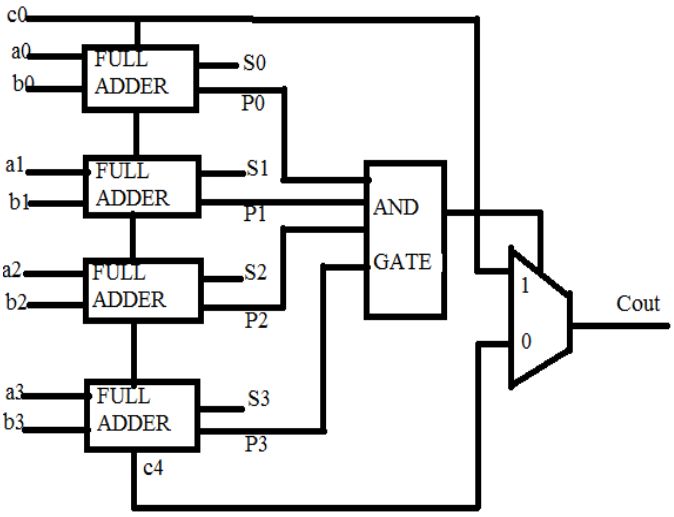

Fig.4: 4-Bit Carry Skip Adder

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III. PROPOSED MODEL

The Heterogeneous adder architecture is proposed and designed with the help of different Homogeneous adder architecture.

The proposed technique is 16-bit Heterogeneous adder and it is concatenation of 8-bit Ripple carry Adder (RCA), 8-bit Carry look ahead Adder (CLA). It will be compared with the 16-bit Homogeneous adder in terms of power, area and delay.The block diagram of the 16-bit Heterogeneous adder is shown below

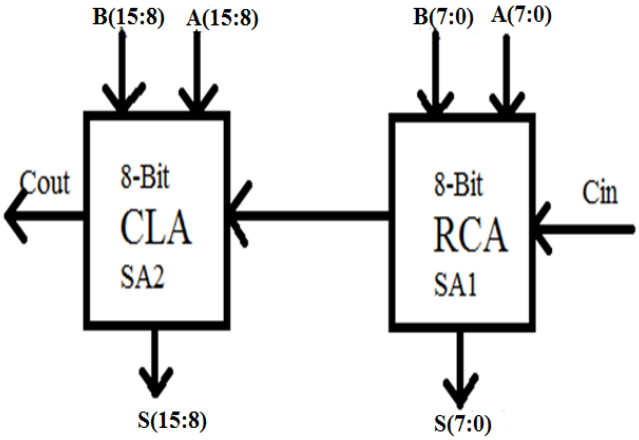

Fig.5: 16-Bit Heterogeneous Adder

IV. RESULTS

1. *Simulation Result for Proposed Model*

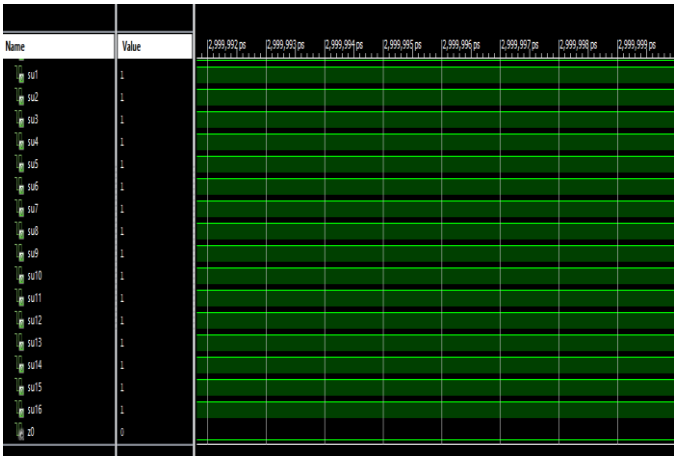

Fig.6: Simulation Results of Proposed Heterogeneous Adder

2. *Schematic Diagram for Proposed Model*

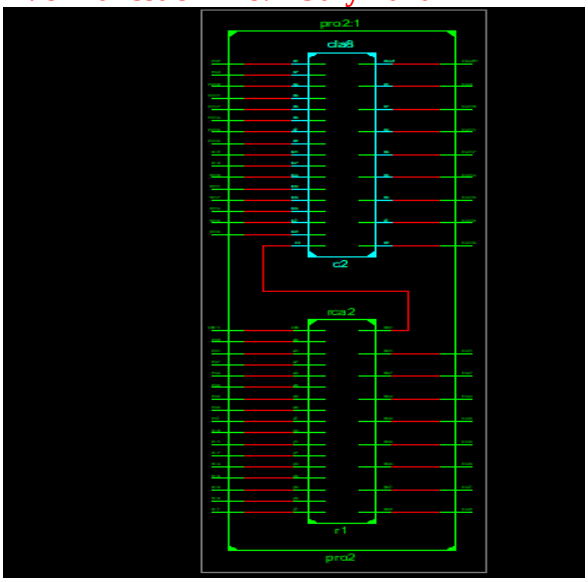

Fig.7:Schematic Diagram for Proposed Heterogeneous Adder

V. COMPARISON AND TABULATION

	8-Bit RCA	8-Bit CLA	Heterogeneous Adder	Homogeneous Adder
Slice LUTs	8	17	25	38
Bonded IOB	25	25	50	50
Utilisation %(LUT)	0.01	0.02	0.02	0.02
Utilisation %(IO)	8.67	8.67	14.67	16.67

Table 1:Comparison of Utilisation between 8-Bit RCA,8-Bit CLA, Heterogeneous Adder, Homogeneous Adder

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	8-Bit RCA	8-Bit CLA	Heterogeneous Adder	Homogeneous Adder
On-chip Memory	5.43w	5.60w	11.07w	12.03w
Junction Temperature	34.6'c	35.6'c	50.3'c	53.6'c
Thermal Margin	64.4'c	49.4'c	43.7'c	44.7'c
Signal (Data)	0.07w	0.17w	0.276w	0.367w
Logic	0.02w	0.05w	0.083w	0.096w
I/O	5.76w	5.28w	10.98w	11.96w

Table 2:Comparison of PowerSummary between 8-Bit RCA,8-Bit CLA, Heterogeneous Adder, Homogeneous Adder

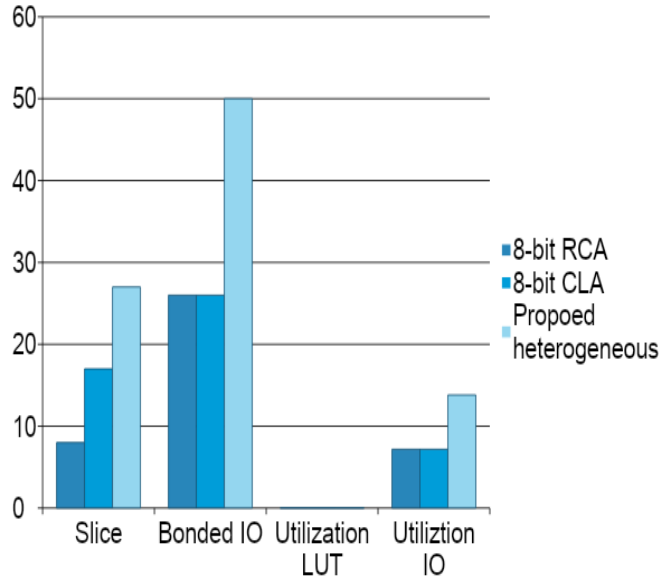

Fig.8: Comparison Graph of Utilization of Heterogeneous Adder

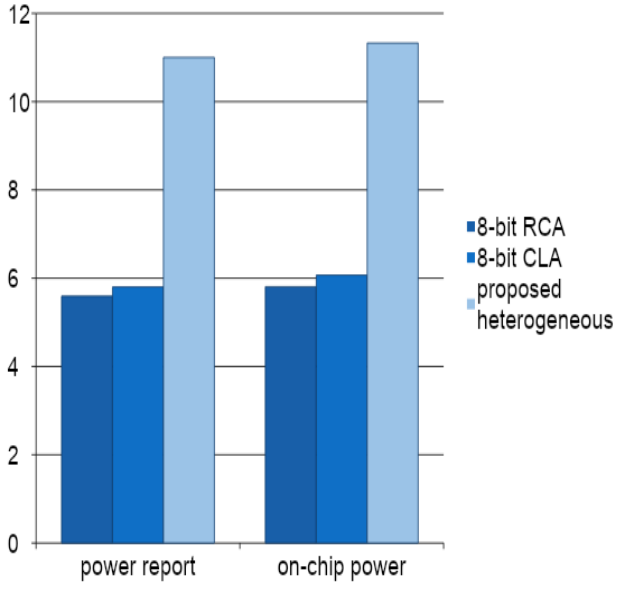

Fig.9: Comparison Graph of Power consumption in Heterogeneous Adders

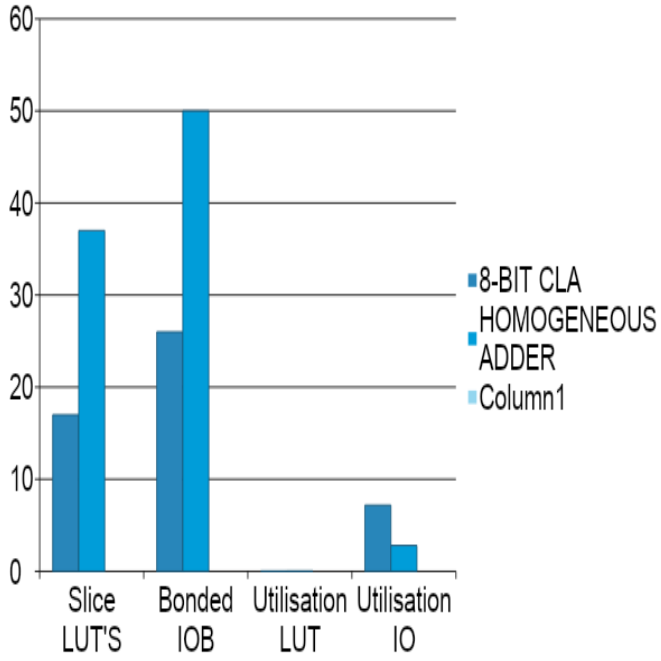

Fig.10: Comparison Graph of Utilization of Homogeneous Adder

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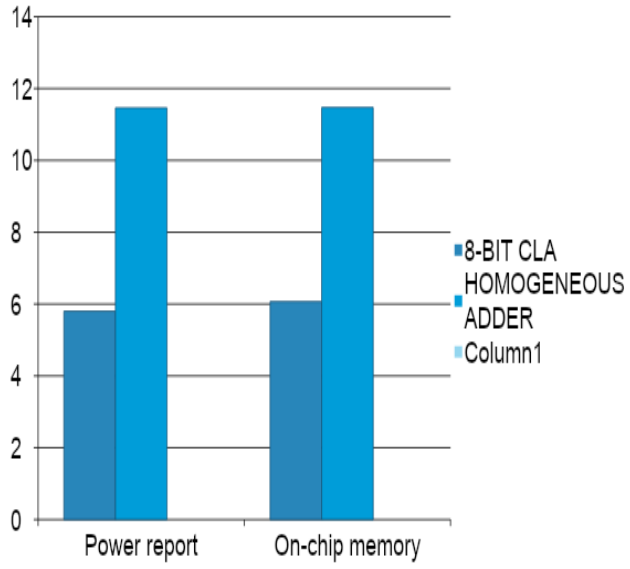

Fig 11: Comparisongraphof powerconsumptionin homogenous adder

VI.CONCLUSION

This paper introduces the Heterogeneous adder using 8-Bit Ripple Carry Adder and 8-Bit Carry Lookahead Adder and it's modeling and simulation according to its properties using VHDL in VIVADO. Thismodel has less thermalmargin under power consumption. It has minimum area and delay which provesto be an easy solution in improving speed of an adder circuit. The respective utilization and powersummary of the proposed model 16-Bit Heterogeneous adder and 16-Bit Homogeneous adder wascompared using Bar- Graph.

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