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THE INTEGRATION OF CRYSTALLINE PR2O3 HIGH-K GATE MATERIAL ADOPTION OF CONVENTIONAL CMOS FABRICATION PROCESSES

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ABSTRACT

In this project work I report on methods to introduce crystalline rare-earth (RE) oxide with high (k>3.9) dielectric constants (high-k) in a CMOS process flow. Key process steps compatible with crystalline praseodymium oxide(pr_20_3) high–k gate dielectric have been developed and evaluated in metal –oxide semiconductor(MOS) structure and n-MOS transistors fabricated in an adapted conventional bulk process. From the capacitance-voltage measurements a dielectric constant of K=36 has been calculated. Furthermore an alternative process sequence suitable for the introduction of high-k material into silicon on insulator(SOI) MOS-field effect transistors(MOSFET) is presented. The feasibility of this process is shown by realization of n-and p-MOSFETs with standard Sio2 gate dielectric as demonstrator sio2 gate dielectric can be replaced by crystalline RE-oxide in the next batch fabrication. Finally, MOSFET is designed in COMSOL metaphysics and simulation results are compared different gate lengths.

Keywords: MOSFET, High k gate dielectric material, praseodymium(Pr2O3), Fabrication, Gate first approach.

Introduction

The advance in complexity and efficiency of CMOScircuits has been achieved throughout the last decadesby scaling the geometric dimensions of the metaloxidesemiconductor field-effect-transistor (MOSFET)[1]. Reducing the gate length increased drive currentswhile it also necessitates a decrease of the gate oxidethickness to maintain electrostatic control of the chargesinduced in the channel [1]. Today the requirement forgate equivalent oxide thickness (EOT) is below 2nmeven for low operating power applications [2]. In thisregime a further reduction produces an exponentialincrease of direct tunneling leakage currents posing afundamental limit for further scaling [3]. A solution toovercome this scaling limit of silicon dioxide (SiO2) asgate insulator is its substitution by crystalline rare-earth(RE) oxides with larger dielectric constants [4]. TheseRE oxides, deposited by molecular beam epitaxy(MBE), have lower leakage currents than silica as wellas temperature stability suitable for CMOS processingand thus appear to be promising candidates for high-kintegration.However any new gate material must be investigatedon devices with a complete process sequence includingwet chemical cleaning, structuring by reactive ion etching(RIE) and high-temperature treatment up to1000 _C. Here we present an approach of introducingcrystalline praseodymium (Pr2O3) high-k material intoa conventional silicon process. First, key process stepsnecessary for device fabrication have been adoptedand MOS capacitances as well as n-MOSFETs havebeen fabricated and their properties measured. Furthermore,an alternative process sequence for the functionalevaluation of crystalline high-k dielectrics in MOSFETson SOI, derived from the process considerations gainedon silicon, is presented. It provides a planar surfaceessential for epitaxial growth of the gate stack prior tothe device isolation and is therefore called a _gatfirst_process.
Experimental results for n- and p-MOSFETswith SiO2 gate material fabricated with this _gate-first_process are presented.

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Microelectronics

Microelectronics is fundamentally a question of electronics chips and of the way to reduce their dimensions improving their performances. Trying to understand the route done in this field, we can mention that 50 years ago a small company called Intel released the 4004, its first ever microprocessor. This chip was immediately perceived as a sort of the eighth wonder of the world considering that the chip, measuring 12 mm^2, contained 2300 transistors. The distance between each transistor was around 10 μm. This is quite small, but always "thinkable" from a human point of view considering that with a small microscope they could be visible. Now if we take into account the transistors on one of the last Intel architecture, the Sky lake chips, released by Intel in 2015, we observe that the chips themselves are 10 times the size of the 4004, but considering that the space between them is only 14 nm, definitively their transistors are invisible for common no sophisticated measurement technique considering that these are around five times bigger than DNA molecules. This short history shows how the paradigm shift from micro to nano has strongly influenced electronics and the way to conceive it. This last has been forecast, up to now, by the Moore's law. But what is indeed the Moore's law and why it is so often quoted? Gordon Moore was the cofounder of Fairchild Semiconductor and Intel, whose 1965 seminal paper described a doubling every year in the number of components per integrated circuit and projected that this rate of growth would continue for at least another decade.

Microelectronics is a subfield of electronics. As the name suggests, microelectronics relates to the study and manufacture (or micro fabrication) of very small electronic designs and components. Usually, but not always, this means micrometer-scale or smaller. These devices are typically made from semiconductor materials. Many components of normal electronic design are available in a microelectronic equivalent.

LITERATURE SURVEY

The application of FET as a biosensor for label-free detection of charged biomolecules has seen significant usage [1-3]. The use of the concept of dielectric modulation of a vertical nanogapin the FET's gate due to the presence of biomolecules has enabled the application of FET biosensors for detecting the presence of charge-free biomolecules as well [4-8]. The reported dielectric-modulated FET (DMFET) based biosensors show high responsiveness to both dielectric modulation and charge of the biomolecules, with the two effects often affecting the device parameters in opposite directions leading to reduced sensitivity [8]. In addition, the DMFET shows a sharp dependence of the sensitivity of biomolecule detection to the nanogap length and a significant fall in sensitivity for short channel lengths [8]. In this letter, we propose, for the first time, the application of impact-ionization MOS (I-MOS) transistor as a bio-sensor. A conventional I-MOS is a gated p-i-n diode, with the gate voltage modulating the channel inversion charge and causing the drain-source voltage to appear across the intrinsic region outside the gate region [9, 10]. On reaching a critical value, the electrical field in the intrinsic region causes impact- ionization leading to an abrupt turning-ON of the I-MOS transistor [11, 12]. Recent results have shown a sub-threshold slope as low as 2-10 mV/dec [13-15].

Biosensing element is the other crucial factor that needs to be taken into account in designing FET biosensors. In the dawn of these FET-based devices, antibodies and DNAs/RNAs are prevailing candidates mainly because they are simple, low-cost to synthesize, can be immobilized on a wide range of various surfaces and provide fast detection via high specificity and affinity binding with the target molecules, which are usually protein and nucleic acids in most of biomedical applications. Nevertheless, on one hand, not only is synthesizing antibodies from animals expensive and inappropriately commercialized but also coverage of immobilization areas is far less than full due to stearic hindrances from bulky structure of antibodies [61]. On the other hand, DNA and RNA probes require high ionic strength conditions to shield their intermolecular repulsive force for hybridizations [24].

Both of them weaken or mislead detected signal by FETs in physiological environments with high screening effect (also known as Debye length). Besides, guanine–cytosine-rich sequences on nucleic

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acid structures, which form stem-loop structures as well as self- and cross-dimers, also contribute to false detection results from nonspecific binding [62]. The subsequent periods thus have witnessed an exploration of new generations including antibody fragments (Fab, Fab' and scFv), aptamers, peptide nucleic acids (PNA), locked nucleic acids (LNA) and neutralized DNA (nDNA) as bio-probes in order to subjugate these drawbacks. .

COMSOL MULTIPHYSICS

Computer simulation has become an essential part of science and engineering. Digital analysis of components, in particular, is important when developing new products or optimizing designs. Today a broad spectrum of options for simulation is available; researchers use everything from basic programming languages to various high-level packages implementing advanced methods. Though each of these techniques has its own unique attributes, they all share a common concern: Can you rely on the results? When considering what makes software reliable, it's helpful to remember the goal: you want a model that accurately depicts what happens in the real world. A computer simulation environment is simply a translation of real-world physical laws into their virtual form. How much simplification takes place in the translation process helps to determine the accuracy of the resulting model. It would be ideal, then, to have a simulation environment that included the possibility to add any physical effect to your model. That is what COMSOL is all about. It's a flexible platform that allows even novice users to model all relevant physical aspects of their designs. Advanced users can go deeper and use their knowledge to develop customized solutions, applicable to their unique circumstances. With this kind of all-inclusive modeling environment, COMSOL gives you the confidence to build the model you want with real-world precision. Certain characteristics of COMSOL become apparent with use. Compatibility stands out among these. COMSOL requires that every type of simulation included in the package has the ability to be combined with any other. This strict requirement actually mirrors what happens in the real world. For instance in nature, electricity is always accompanied by some thermal effect; the two are fully compatible. Enforcing compatibility guarantees consistent multiphysics models, and the knowledge that, even as the COMSOL family of products expands, you never have to worry about creating a disconnected model again. Another noticeable trait of the COMSOL platform is adaptability. As your modeling needs change, so does the software. If you find yourself in need of including another physical effect, you can just add it. If one of the inputs to your model requires a formula, you can just enter it. Using tools like parameterized geometry, interactive meshing, and custom solver sequences, you can quickly adapt to the ebbs and flows of your requirements. 6 | Introduction COMSOL Multiphysics also has several problem-solving benefits. When starting a new project, using COMSOL helps you understand your problem. You are able to test out various geometrical and physical characteristics of your model, so you can really hone in on the important design challenges of the COMSOL environment facilitates further analysis

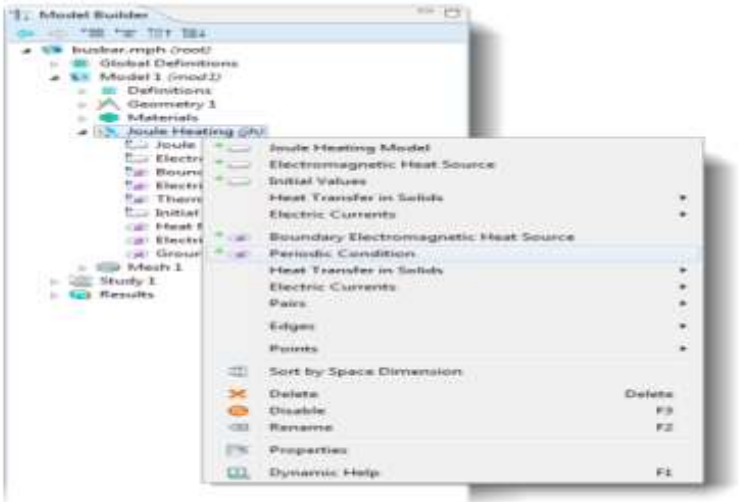

Fig: Model tree

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When you right-click any node in the tree, a context menu shows the available features. In addition, many nodes can be easily moved up and down in the model tree by dragging and dropping the nodes. You can also right-click to copy, delete, disable, or enable nodes.

If you choose an action that requires specification, the matching settings window displays next to the Model Builder: Click any associated node to return to a specific settings window. As you create the model, each step is shown in the Model Builder. If, for example, your model required a certain sequence of steps to get the right geometry, these are all listed in the order you set.

This series of steps can be edited and rerun without having to repeat the entire simulation. Complicated solver sequences you may need for different studies also benefit greatly from this feature. As you work with the COMSOL Desktop and the Model Builder, you will grow to appreciate the organized and streamlined approach. But any description of a user interface is inadequate until you try it for yourself. So in the next few sections, you are invited to work through some examples to familiarize yourself with the software.

Thorough Example: The Busbar Electrical Heating in a Busbar In order to get acquainted with COMSOL Multiphysics, it is best to work through a basic example step by step. These instructions describe the essential components of the model building procedure, highlighting several features and demonstrating the common simulation tasks. At the end, you will have built a truly multiphysics model. The model that you are about to create analyzes a busbar designed to conduct direct current to an electric device (see below). The current conducted in the busbar,

from bolt 1 to bolts 2a and 2b, produces heat due to the resistive losses, a phenomenon referred to as Joule heating.

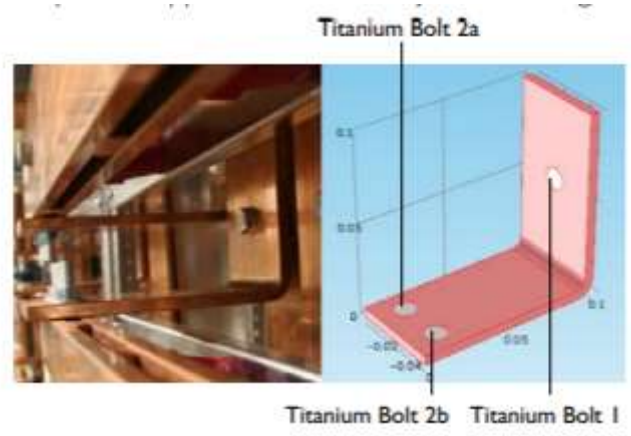

Fig: Bus bar

The busbar is made of copper while the bolts are made of a titanium alloy. The choice of materials is important because titanium has a lower electrical conductivity than copper and will be subjected to a higher current density. The goal of your simulation is to precisely calculate how much the busbar heats up. Once you have captured the basic multiphysics phenomena, you will have the chance to investigate thermal expansion yielding structural stresses and strains in the busbar and the effects of cooling by an air stream. The Joule heating effect is described by conservation laws for electric current and energy. Once solved for, the two conservation laws give the temperature and electric field, respectively. All surfaces, except the bolt contact surfaces, are cooled by natural convection in the air surrounding the busbar. You can assume that the bolt cross-section boundaries do not contribute to cooling or heating of the device. The electric potential at the upper-right vertical bolt surface is 20 mV, and that the potential at the two horizontal surfaces of the lower bolts is 0 V.

PROPSED METOD:

‘Gate-first’ approach:

This section describes a concept to integrate crystallinehigh-k Pr2O3 into a CMOS process on SOI substrates.SOI CMOS technology offers superior speed and power performance compared to silicon and is commonlyused by major chip manufacturers . However,the conventionally used way of mesa isolation leads tostructured non-planar surfaces before the gate dielectricis deposited . Such a process

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flow is therefore notsuitable for MBE growth of a crystalline dielectric.The _gate-first_ approach complies with this criterionby a changed process flow. It is developed here using astandard SiO2 gate dielectric that can be replaced by anyMBE high-k dielectric.

Device concept and fabrication:

In the _gate-first_ approach, the planar gate stack isformed prior to device isolation, similar to the EXTIGATEprocess used for silicon wafers. This providesa silicon surface necessary for MBE of an epitaxial crystallinelayer. An overview of the gate-first process flow isgiven in Fig. 6. The initial SOI substrate with 100 nmtop-silicon on 200 nm buried oxide (BOX) is doped byion implantation to obtain n- and p-MOS transistors.The channels are doped with boron to NA = 6 ·1017 cm_3 and arsenic to ND = 6 · 1017 cm_3, respectively.Rapid thermal annealing is done in inert atmosphereat 1100 _C for 4 min. After an RCA clean, athermal oxide with a thickness of tox = 8 nm is grownat 900 _C. Subsequently, polysilicon with a thicknessof tpoly = 150 nm is deposited by low pressure chemicalvapour deposition (LPCVD) to complete the planargate-stack on SOI.The polysilicon layer is doped by ion implantationwith arsenic and boron to N = 3 · 1020 cm_3 to serveas n+ and p+ gate electrode, respectively. RTA to activatethe gate dopants is performed at 930 _C for 45 s forn-MOSFETs and 12 s for p-MOSFETs. Optical contactlithography defines a mesa region for source, drain and gate.

Polysilicon, gate oxide and top-siliconare etched in an inductive coupled plasma reactive ion etching system [Oxford Plasmalab 100] (ICP-RIE) with a two stepHBr process . Here, the challenge lies in the formation of an anisotropic etch profile through different materials. A stepped or tapered profile would lead to a conducting path without gate-control. The anisotropic first step with pure HBr at 7 mTorr etches the complete stack down to a remaining thickness of 10 nm top-silicon. The etch rate for polysilicon is 87 nm/min and the etch rate for gate oxide is 12 nm/ min. The top-silicon is etched similar to the polysilicon. The second etch step with HBr 60 mTorr removes the remaining top-silicon with an etch selectivity >200 to the underlying BOX. A consecutive optical lithography then defines the polysilicon gate . The following RIE step uncovers the source- and drain regions . This process again uses HBr and is carried out at 60 mTorr to stop on the gate oxide and to avoid abrasion of the BOX around the mesa structure. The gate oxide above source and drain regions is removed with an HF-dip (5%) . Source and drain contacts are formed by a self-aligned ion implantation with arsenic and boron to a dose of N = 3e20/ cm3, followed by RTA at 930 _C for 45 s and 12 s, respectively. The transistors are completed by a 30 min forming gas anneal at 400 _C.

The proposed model have a very narrow dielectric layer giving a room for the Bio-lipd to occupy the space and modulate the dielectric constantof the layer. The altered dielectric constant results in different ID.The ID is calibrated to identify the isue

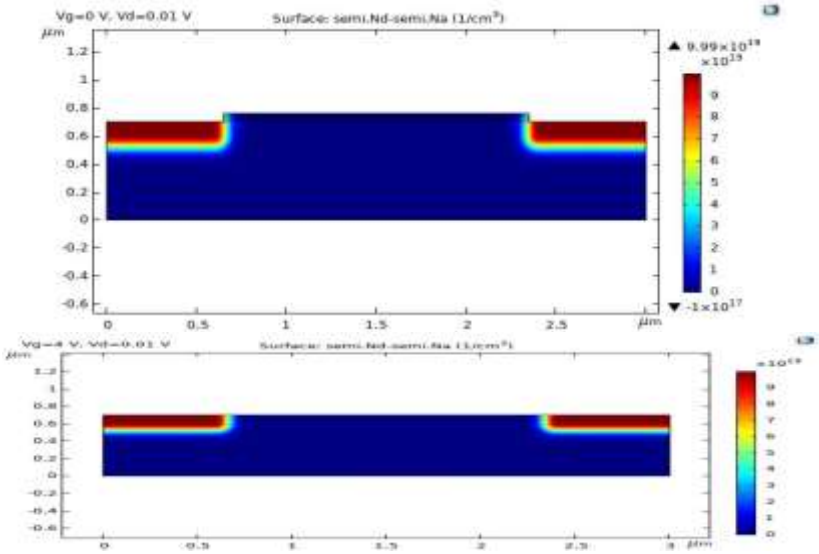

Fig:Proposed method

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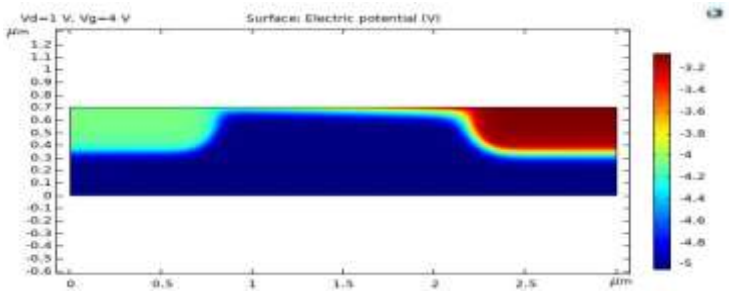
In the proposed method first we are forming the drain and source which are indicated in red colour in the diagram. In the middle of the drain and source we are replacing Sio2 with Pr2o3. A polysilicon is used which is having god reaction properties and is used as an adhesive or gum to strongly attatch Pr2o3 with channel.



RESULT:

Electrical measurements have been performed on n+polysilicon/Pr2O3/silicon capacitances. From the accumulationregime of the high-frequency capacitance–voltage (HF-CV) curve in Fig. 1 we calculate (parallelplate capacitor) a dielectric constant of k = 36 and an equivalent oxide thickness of EOT = 1.8 nm for a Pr2O3 thickness of 17 nm measured by ellipsometry.

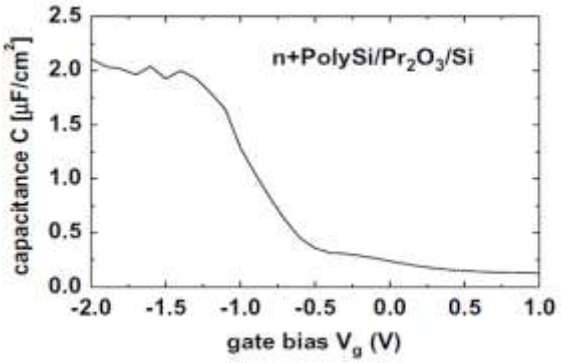


Fig: C-V curve of n+polysilicon /Pr2O3 MOS structures

Admittance measurements have been performed toderive the equivalent parallel conductance shown inFig. 2. The interface trap density, Dit = 3.5 · 1011/cm2eV, has been calculated from the peak conductance[8].This high density indicates that further interfaceengineering is needed to achieve quality levels comparable.

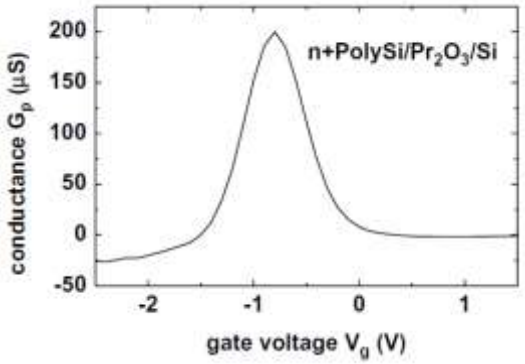


Fig: Results of conductance measurements of n+polysilicon/Pr2O3 MOS structures

n-MOSFETs

Measurements on n-MOSFETs show fully functional transistor behavior as shown by the output characteristics as shown in fig. A test device with a gate length ofLg = 4 lm and a gate width of W = 100 lm turns onproperly. From the transfer characteristics a threshold voltage of Vth = 1.6 V has

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been determined.This is larger than the Vth = 0.6 V obtained for a comparabletransistor with SiO2 gate dielectric. This threshold voltage shift is caused by a substantial amount ofnegative oxide charges. The sub-threshold swingof S = 145 mV/dec also indicates a high number of interface charges, which degrades the switching performance.An analysis of the gate leakage current of n-MOSFETs is showing in fig for gate bias sweeps from 0 V.

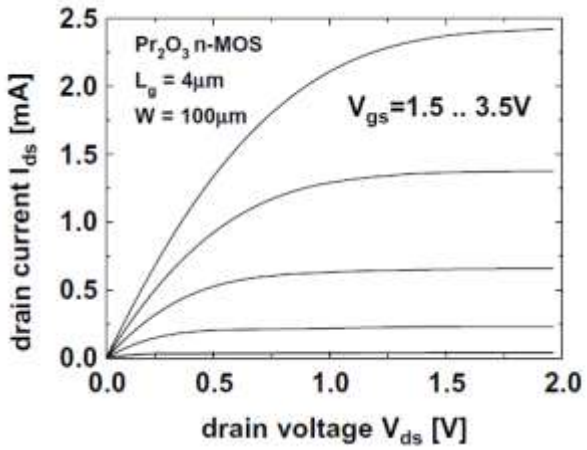

Fig: Out put characteristics of n MOSFET with polysiliocon/Pr2O3 gate stack

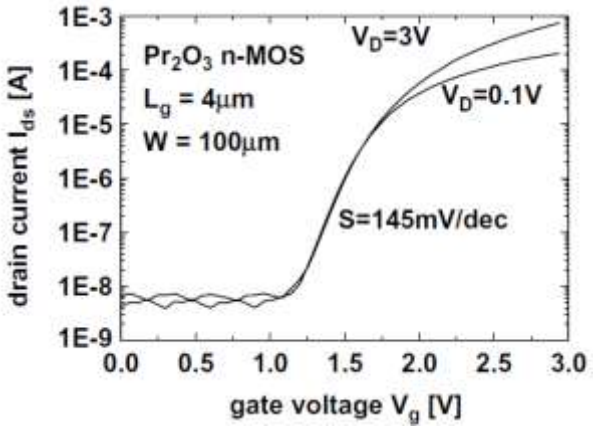

Fig: Transfer characteristics of nMOSFET with polysilicon/Pr2O3 gate stack

CONCLUSION

I have successfully demonstrated the feasibility of integrating high-k gtae dielectric praseodymium oxide(Pr2O3) in a CMOS process. In the first part of this work the compatibility of Pr2O3 with critical CMOS process steps have been investigated in detail and alternative solutions are suggested for those processes found incompatible. In the second part, a novel-gate-first-process for silicon-on-insulator technology is presented. Devices fabricated with this concept have proper MOSFET characteristics. The combination of the Pr2O3 results with –gate-first-approach allows simple introduction of novel high-k materials grown by molecular beamepitaxy in to advanced SOI devices.

FUTURE SCOPE

The character of interactions between the dielectric film and the dopant atoms in the substrate remains to be investigated. Resistance of the dielectric against the unwanted boron diffusion from the poly gate to the substrate is an issue which may be of importance atleast in the first practical implementations of high-k gate oxides .It is not yet clear if any “Si friendly” high-k dielectric can be found. Recently,many promising candidates,including metal electrodes have been identified and

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some preliminary prototype field effect transistor produced.The grand challenge involves identifying the appropriate dielectric that fulfills all material requirements and can be successfully implemented in to CMOS in a cost-effective manner.

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