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Designing of 21-Level Cascaded H-Bridge converter usingSVM technique

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ABSTRACT:

The proposed topology significantly reduces the number of dc voltage sources, switches, IGBTs, and power diodes as the number of output voltage levels increases. To synthesize maximum levels at the output voltage, the proposed topology is optimized for various objectives, such as the minimization of the number of switches, gate driver circuits and capacitors, and blocking voltage on switches. This new type of converter is suitable for high voltage and high power applications. This multilevel inverter has ability to synthesize waveformswith better harmonics spectrum. In this project a study of 21-level inverter using less number of switches as compare to the technologies previously developed. MATLAB software is used for simulate the 7-level inverter. Also a comparison analysis is carried out for symmetrical and asymmetrical multi-level inverter with open loop as well as closed loop using PI controller. The simulation was carried out using MATLAB/Simulink. The simulation study demonstrates the merits of asymmetrical multi-level inverter over symmetrical multi-level inverter and also proves the effectiveness of closed loop PI controller in providing an output voltage with reduceddistortions.

Introduction:

Multi-level inverters are broadly utilized as a part of high power applications because of its momentous merits over customary two level inverters, for example low switching losses, better electromagnetic capability, and lower harmonics. Comparing two-level inverter topologies at the same power ratings, MLIs additionally have the favorable circumstances that the harmonic components of line-to-line voltages connected to load are decreasedowing to its switching frequencies. Plenty of multi-level inverters are proposed however, still most popular MLI configurations are Neutral point clamped MLI, flying capacitor MLI, Cascaded H-Bridge MLI (CHBMLI). Among all the above mentioned inverters Cascaded H-Bridge multi-level inverters are mainly preferred in most of the researches especially dealing non-conventional energy sources like Photovoltaic and Fuel cell. Because, the cascaded inverter has the least components for a given number of levels. Cascade multilevel inverters consists of a series of H-bridge cells to synthesize a desired voltage from several separate DC sources which might be acquired from PV cells, batteries or fuel cells. All these features of cascade inverters allow using various pulse width modulation (PWM) strategies to control the inverter accurately. Cascaded H-Bridge MLI's are of two types symmetrical and asymmetrical topologies. Unlike symmetrical MLI, the asymmetrical MLI structure involves unequal DC sources. The symmetrical CMLI and asymmetrical CMLI topologies for a 7 level output voltage areshown in fig.1.

There are various modulation strategies for providing pulses to the switches of multi-level inverters. An efficient approach to control the asymmetrical MLI is multi carrier PWM technique in which the high frequency

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carrier wave (triangular) is compared with low frequency reference wave (sinusoidal). Multi carrier modulation is realized with two techniques namely phase shifted and level shifted techniques. Again level shifted modulationis divided into phase disposition (PD), Phase opposition disposition (POD), and Alternate phase opposition disposition (APOD).

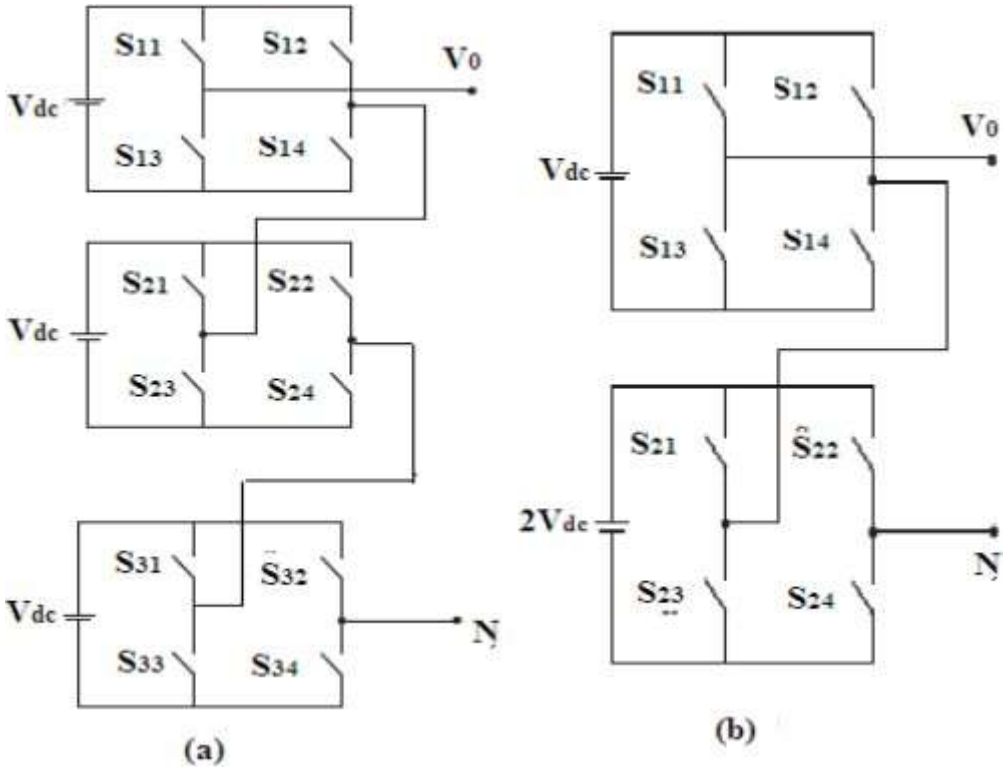

Figure 1: Seven level CHBMLI topologies (a) Symmetrical b) Asymmetrical

H-BRIDGE INVERTER

"H" topology has many redundant combinations of switches' positions to produce the same voltage levels. As an example, the level "zero" can be generated with switches in position S(1) and S(2), or S(3) and S(4), or S(5) and S(6), and so on. Another characteristic of "H" converters is that they only produce an odd number of levels, which ensures the existence of the "0V" level at the load. For example, a 51-level inverter using an "H" configuration with transistor-clamped topology requires 52 transistors, but only 25 power supplies instead of the 50 required when using a single leg. Therefore, the problem related to increasing the number of levels and reducing the size and complexity has been partially solved, since power supplies have been reduced to 50%.

In this case, the power supply could also be voltage regulated dc capacitor. The circuit diagram consists of two cascade bridges. The load is connected in such a way that the sum of output of these bridges will appear across it. The ratio of the power supplies between the auxiliary bridge and the main bridge is 1:3. One important characteristic of multilevel converters using voltage escalation is that electric power distribution and switching frequency present advantages for the implementation of these topologies.

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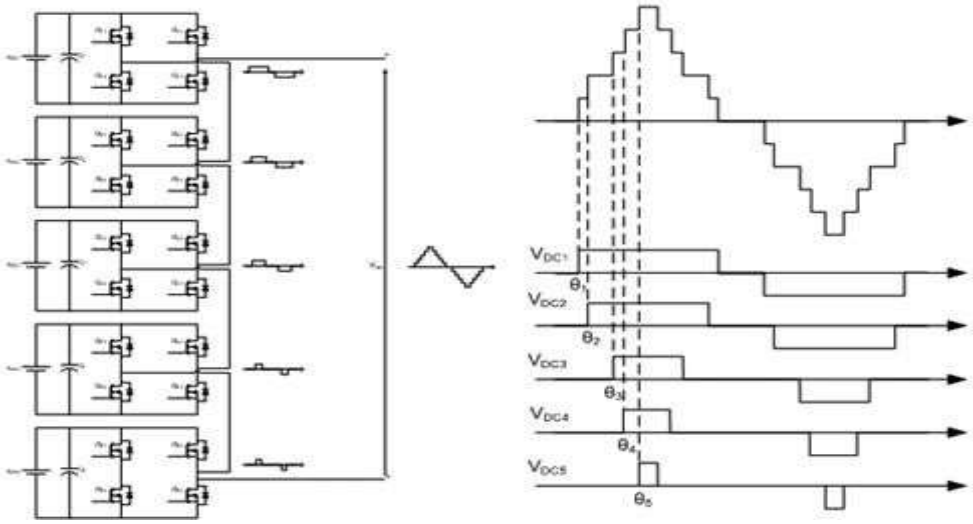

Figure 2: Cascade H-Bridge Multilevel Inverter

Space Vector Modulation Technique:

A different approach for getting gate triggering signals instead of general pulse width modulation technique is based on the space vectors generated by the system two phase vector components d, q axis.

Fig: 3 shows the space vector representation of the adjacent vector V1 and V2 with 8 space vector switching pattern positions of inverter as shown in figure.

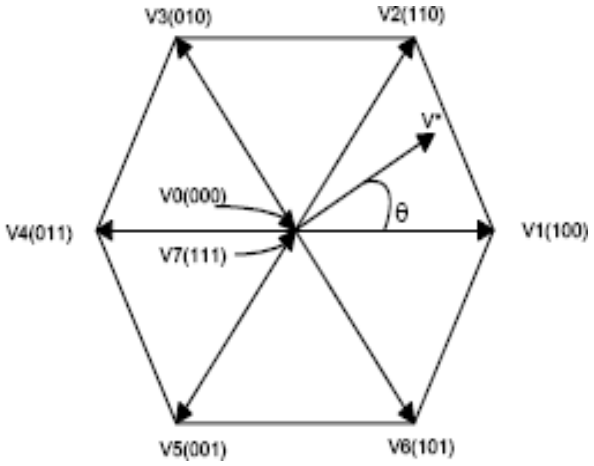

Fig 3: Space Vector Modulation Technique

Generally, the Space Vector Modulation Technique is one of the most popular and important technique in pulse width modulation methods of the three phase voltage source inverters for technique, we get the less harmonics in the both output voltage and output currents of the applied ac motors. The space vector modulation technique is used in this paper for creating the reference vectors generated by modulating the switching time sequence of space vectors in each of six sectors as shown in figure 3. From figure 3, six switching sectors are used for inversion purpose and two sectors are behave like a null vectors.

Space vector modulation can be implemented by the following procedures:

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1. Transformation of three phase quantities into two phase quantities.

2. Determine time duration T1, T2 and T0.

The reference signals for voltages and V0 to V7 and switching time sequences are generated by the following expression

V* Tz = V1 *T1 + V2 *T2 + V0 *(T0/2) + V7 *(T0/2)

INDUCTION MOTOR

In this paper, the induction motor is considered as electric motor for EVS. Because of its high- performance, cheap cost good speed regulation and absence of commutation and also the control of induction motor drive of industrial applications and automation based production has received wide spread research interests. In induction motor 3-phase AC supply is apply to stator, it develop the RPM. The rotor establishes the induced currents due to inter action between RMF and stationary rotor. These induced currents produces magnetic field and rise to uni-directional torque. Figure 3 shows the equivalent representation of induction motor in electrical.

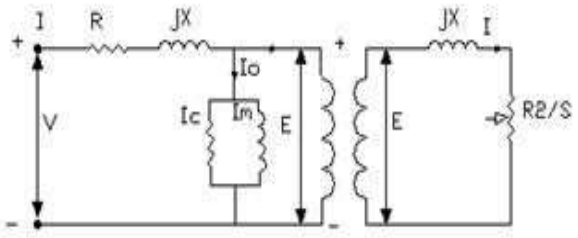

Figure 4: Steady state Equivalent circuit of an induction motor

Simulation Diagram and Analysis:

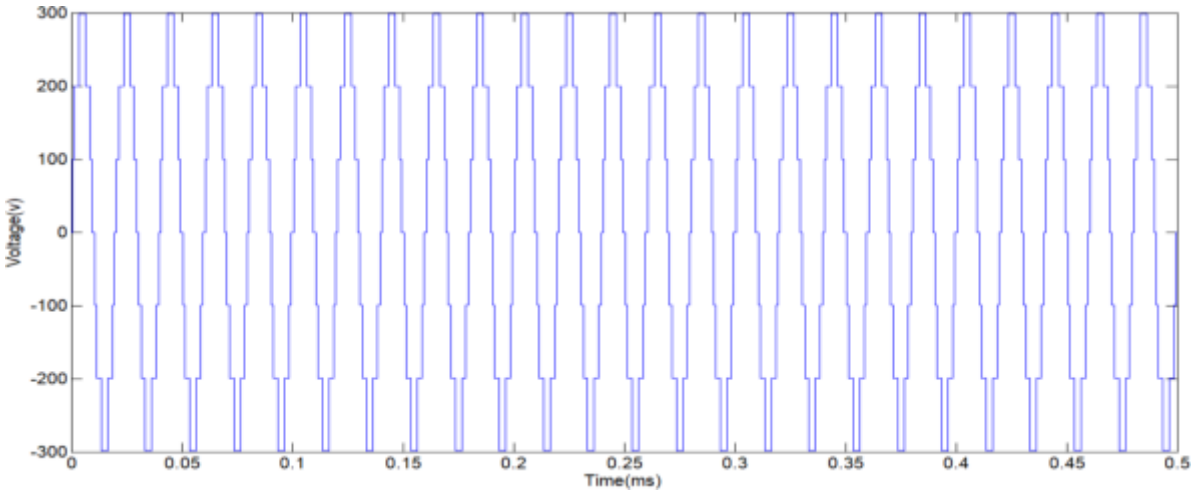

Figure 5: Simulation Waveform for 7-Level MLI

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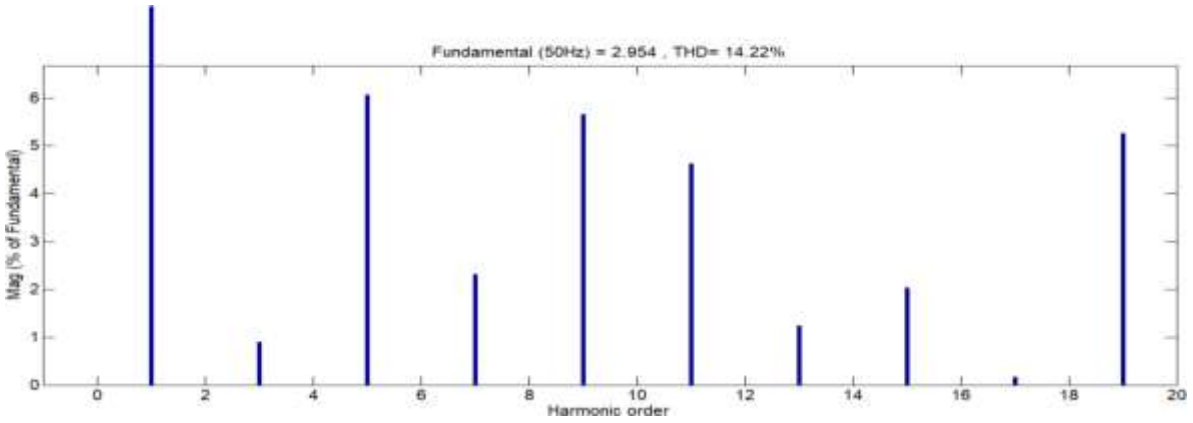

Figure 6: Simulation THD

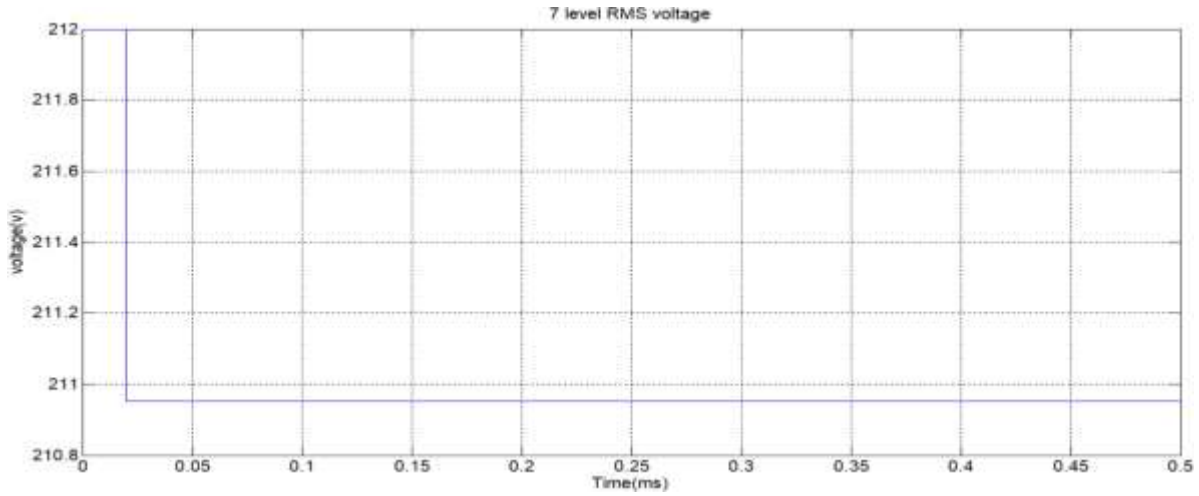

Figure 7: Simulation RMS Waveform for 7-Level MLI

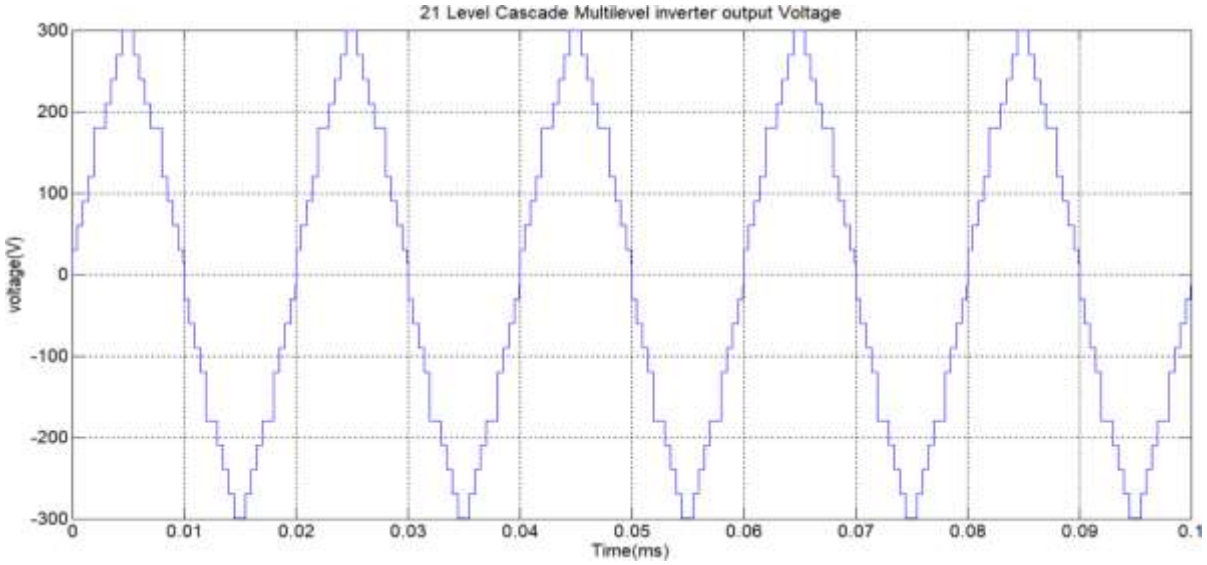

Figure 8: Simulation Waveform for 21-Level MLI without Filter

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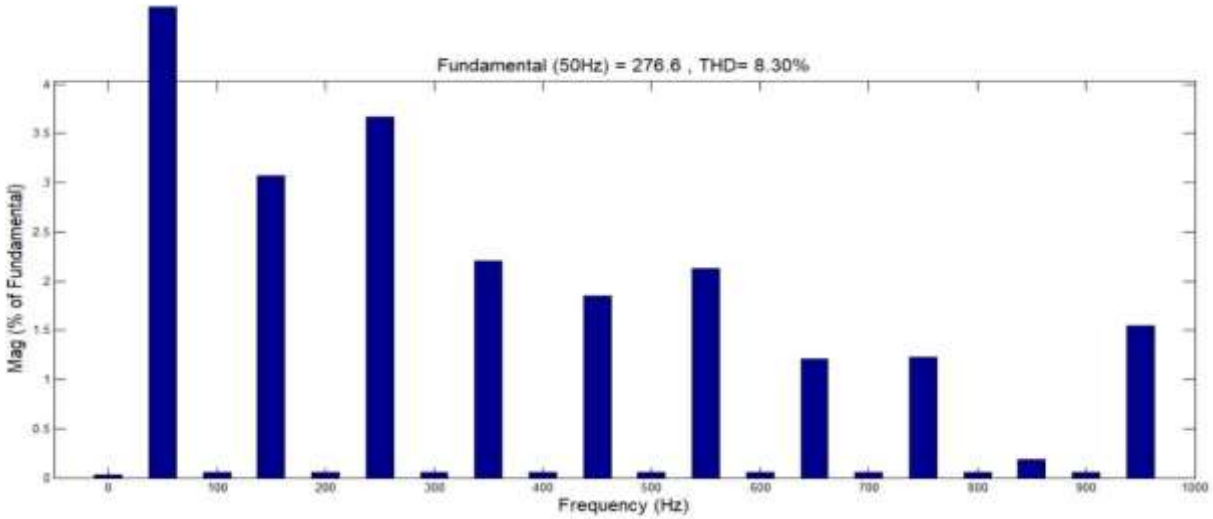

Figure 9: Simulation voltage THD without filter

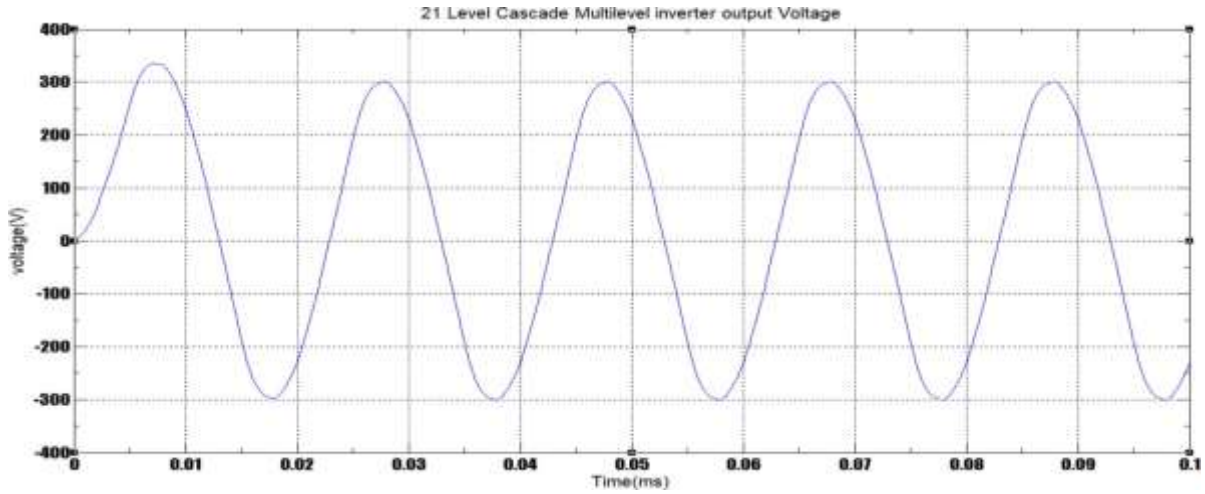

Figure 10: Simulation Waveform for 21-Level MLI with Filter

CONCLUSION

As the presented topology consists of the cascaded basic units. The proposed basic unit and the proposed multilevel inverter uses lower number of switching devices and gate driver circuits, the proposed topology considers two design parameters. They are the number of cascaded basic units and the number of dc voltage sources in each basic unit. These two parameters can be used to design the desired multilevel converter based on the operational conditions. Thus, the proposed topology offers good flexibility in designing. The simulation results obtained in MATLAB/Simulink as well as the experimental results of a 21-level Inverter based on the proposed topology are presented to verify its performance. Multilevel Inverters generate stepped output voltage by a proper arrangement of power electronic switches and several dc voltages sources. As the number of output voltage levels increases, the output voltage becomes more identical to a sinusoidal waveform resulting in lower distortions. Multilevel Inverters have some advantages in comparison with the conventional two-level Inverters and the other previous proposed topologies including the use of low-voltage power electronic switches and improved output voltage quality. This results in the lower stress on the power electronic devices, lower losses and produces betterharmonic levels. The results have been presented and analysed.

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