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A NOVAL METHOD TO DESIGN 3-BIT BURST ERROR-CORRECTION CODES WITH QAEC

K. Adi Narayana[1], K. Bhaskar Reddy[2], M. Ramesh Naidu[3]
[1]*Assistant Professor,* [2]*Assistant Professor,* [3]*Associate Professor, ECE Department, Anantha Lakshmi Institute of Technology and Sciences, Ananthapuramu, Andhra Pradesh, India.*

ABSTRACT*--The use of error-correction codes (ECCs) with advanced correction capability is a common system-level strategy to harden the memory against multiple bit upsets (MBUs). Therefore, the construction of ECCs with advanced error correction and low redundancy has become an important problem, especially for adjacent ECCs. Existing codes for mitigating MBUs mainly focus on the correction of up to 3-bit burst errors. As the technology scales and cell interval distance decrease, the number of affected bits can easily extend to more than 3 bit. The previous methods are therefore not enough to satisfy the reliability requirement of the applications in harsh environments. In this paper, a technique to extend 3-bit burst error-correction (BEC) codes with quadruple adjacent error correction (QAEC) is presented. First, the design rules are specified and then a searching algorithm is developed to find the codes that comply with those rules. The H matrices of the 3-bit BEC with QAEC obtained are presented. They do not require additional parity check bits compared with a 3-bit BEC code. By applying the new algorithm to previous 3-bit BEC codes, the performance of 3-bit BEC is also remarkably improved. The encoding and decoding procedure of the proposed codes is illustrated with an example. Then, the encoders and decoders are implemented using a 65-nm library and the results show that our codes have moderate total area and delay overhead to achieve the correction ability extension.

Index Terms—Burst error-correction codes (ECCs), ECC, multiple bit upset (MBU), memory, quadruple adjacent error correction (QAEC).

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1.INTRODUCTION

Reliability is an important requirement for space applications [1]. Memories as the data storing components play a significant role in the electronic systems. They are widely used in the system on a chip and application-specific integrated circuits [2], [3]. In these applications, memories

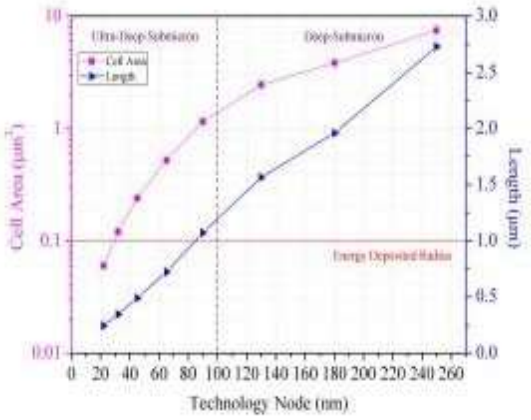

Fig. 1. Memory cell area of different technology (cell area shape is simplified to a square, and Length is the length of side).

account for a large portion of the circuit area [4]. This makes memories suffer more space radiation than other components. Therefore, the sensitivity to radiation of memories has become a critical issue to ensure the reliability of electronic systems. In modern static random access memories (SRAMs), radiation-induced soft errors in the form of the single event upset (SEU) and multiple bit upset (MBU) are two prominent single event effects [5]. As semiconductor technology develops from the sub micrometer technology to the ultra deep sub micrometer (UDSM) technology, the size of memory cells is smaller and more cells are included in the radius affected by a particle [6], [7] as shown in Fig. 1.

When a particle from a cosmic ray hits the basic memory cell, it generates a radial distribution of electron–hole pairs along the transport track [8]. These generated electron–hole pairs can cause soft errors by changing the values stored in the memory cell leading to data corruption and system failure [9]. For the transistors with a large feature size, a radiation event just affects one memory cell, which means that only the SEU occurs. In this case, the use of single error-correction (SEC)- double error-detection (DED) codes [10] is enough to protect the memory from radiation effects.

As the feature size enters into DSM range, the critical charge keeps decreasing and the area of the memory cell scales down for each successive technology node. This makes more memory cells affected by a particle hit as shown in Fig. 2. For the CMOS bulk technology, with the cell-to-cell spacing decreasing, the electron–hole pairs generated

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in the substrate can diffuse to nearby cells and induce MBUs [11]–[14]. This

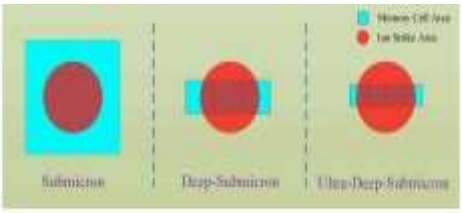

Fig. 2. Schematic description of memory cells included in the radiation effect with variation of the technology node.

compares with the FDSOI technology, which isolates transistors and limits the multi collection mechanism. Therefore, the multi collection mechanism is more prominent for a bulk technology, and the MBU probability is higher [15]–[18]. To protect against MBUs, ECCs that correct adjacent bit errors [19]–[24] or multiple bit errors [25]–[27] are utilized. Although multiple bit error-correction codes (ECCs) can correct multiple bit errors in any error patterns not limited to the adjacent bits, the complexity of the decoding process and the limitation of the code block size limit their use. Meanwhile, from the generation principle of MBUs in [28], the type of the MBUs depends on the initial angle of incidence and scattering angle of the secondary particles. Based on this, adjacent bit errors are dominant error patterns among the multiple bit errors. Therefore, adjacent bits correction ECCs become popular in memory-hardened designs. Many codes are proposed, and the capability of adjacent bits correction mainly focuses on the double adjacent error correction (DAEC) [19]–[22], triple adjacent error correction (TAEC), and 3-bit burst error correction (BEC) [23]. An alternative to codes that can correct adjacent errors is to use an SEC or SEC-DED code combined with an interleaving of the memory cells. Interleaving ensures that cells that belong to the same logical word are placed physically apart. This means that an error on multiple adjacent cells affects multiple words each having only one bit error that can be corrected by an SEC code. As noted in previous studies, interleaving makes the interconnections and routing of the memory more complex and it will lead to an increase area and power consumption or limitations in the aspect ratio [19], [20]. Therefore, whether it is better to use SEC plus interleaving or a code that can correct adjacent errors will be design-dependent and both alternatives are of interest.

2.LITERATURE SURVEY

S. K. Vishvakarma, B. S. Reniwal, V. Sharma, C. B. Khuswah, and D. Dwivedi, "*Nanoscale memory design for efficient computation: Trends, challenges and opportunity*,"[2] The importance of

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embedded memory in contemporary multi-core processors and system-on-chip (SoC) for wearable electronics and IoT applications is growing. Intensive data processing in such processors and SoCs necessitates larger on-chip, energy-efficient static random access memory (SRAM). However, there are several challenges associated with low-voltage SRAMs. In this paper we have discussed the major hurdles at technology front for low power and robust SRAM design. We have discussed the different circuit techniques to mitigate these severe reliability concerns for embedded SRAM. Furthermore, this paper presented the recent development in embedded memory technology targeted to efficient computation. We have analyzed the effect of various device sizing on memory stability. The novel current mode circuit is also presented for high speed, offset tolerant SRAM sense amplifier. The Fin FET memory design is explored to reduce the external manifestation of device mismatch on SRAM stability and memory yield.

4.PROPOSED WORK

BINARY BLOCK LINEAR CODES

In previous works, codes for SEC-DAEC-DED, SEC-DAEC-TAEC, and 3-bit BEC have been proposed. All of them are binary linear block codes. The process used to design these codes is based on some rules for linear block codes construction. In this paper, the proposed codes are also binary linear block codes and obey similar construction rules. Normally, the binary codes are described by the number of data-bits, k, redundancy bits, (n − k), and the block size of the encoded-word, n. An (n, k) code is defined by its generator matrix G or parity check matrix H in

$$G = [P_{k\times(n-k)} \cdot I_{k\times k}] \quad H = [P^T \cdot I_{(n-k)}] \tag{1}$$

where $I_{k\times k}$ is the identity matrix, P is the matrix with size $k \times (n - k)$, and P^T is the transpose of P. In the encoding process, the generator matrix G is used to encode the data bits through the process in

$$v = u \cdot G \tag{2}$$

where $u(u_0, u_1, \ldots, u_{k-1})$ are the data bits to be encoded, and $v(v_0, v_1, \ldots, v_{n-1})$ is the codeword. In the decoding process, the parity check matrix H is used to decode the received codeword through the process in

$$S = r \cdot H^T \tag{3}$$

where $r (r_0, r_1, \ldots, r_{n-1})$ is the received codeword, $S(s_0, s_1, \ldots, s_{n-k-1})$ is the syndrome, and a significant parameter for

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correcting errors. The errors injected into the received code can be described by using

$$r = v + e\ (e0, e1, \ldots, en-1) \quad (4)$$

where e (e0, e1, . . . , en−1) is the error vector indicating that an error occurs in the ith bit when ei = 1. When multiple bit errors occur in the received codeword r with the error vector e = (e0, e1, . . . , en−1), the syndrome of the code considering the error vector in decoding process can be calculated by the method in

$$S = e \cdot HT . \quad (5)$$

This equation formulates the relationship between the syndrome and the corresponding error pattern. Considering the detailed structure of the parity matrix H, when one error occurs in the ith bit, the corresponding syndrome is equal to the ith column vector. When errors occur in the ith bit and the jth bit, the corresponding syndrome is equal to the xor result of the ith column vector and the jth column vector. Therefore, if one error can be corrected or detected, it obeys the following rules.

1) Correctable Restriction: The corresponding syndrome vector is unique in the set of the syndromes.

2)Detectable Restriction: The corresponding syndrome vector is nonzero.

CODE DESIGN TECHNIQUE

In this section, we discuss the code design technique for 3-bit BEC with QAEC. The approach used is based on syndrome decoding and the analysis of the requirements in terms of parity check bits and the formulation of the problem is similar to the one used in some previous studies like [23] and [30]. The process used to design QAEC codes can be divided into error space satisfiability problem and unique syndrome satisfiability. Section III-A explains the error space satisfiability problem, and Section III-B is the unique syndrome satisfiability problem.

A. Error Space Satisfiability

For a code with k data bits and c check bits, its input can represent 2k binary values. If one error occurs, it has k +c bit positions for a single error with output space of (k + c) · 2k values. If adjacent errors occur, it has k + c − 1 bit positions for double adjacent errors with output space of (k+c−1) · 2k values, (k +c−2) bit positions for triple adjacent errors with output space of (k +c −2) · 2k values, . . . , (k +c −(N − 1)) bit positions for N adjacent errors with output space of (k + c−(N −1)) · 2k values. If almost adjacent errors occur, it has (k+c−2) bit positions for errors in 3-bit window with output space of (k + c − 2) · 2k values, (k + c − 3) bit positions for each type of errors in 4-bit window with

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output space of (k + c − 3) · 2k values. To obtain the codes that can correct the errors with certain fault types, the sum of the output space value of error patterns should be less than or equal to the whole output space value 2k+c.

TABLE I
MINIMUM CHECK BIT AND SYNDROME CONDITION

Data Bits	Check Bits	Total Bits	Syndromes Needed	Syndromes Available	Syndromes Left
16	7	23	107	120	13
32	8	40	192	247	55
64	9	73	357	502	145

For the proposed code, to correct 3-bit burst and quadruple adjacent errors, the total condition of the error patterns is (k +c−3)+(k+c−2)+(k+c−1)+(k+c)+(k+c−2), respectively, for quadruple adjacent errors, triple adjacent errors, double adjacent errors, single errors, and 3-bit almost adjacent errors. Based on the error space satisfiability principle, the relation between the space of the correct codeword and the space of the erroneous codeword can be derived from

$$2^k(5(k+c)-8+1) \leq 2^{k+c}. \quad (6)$$

Based on (6), the minimum number of check bits used for 16, 32, and 64 data bits is shown in Table I. Meanwhile, the available syndromes and the ones needed in the best case to correct 3-bit burst and quadruple adjacent error are also shown in Table I.

Here, we should note that the number of parity check bits needed is the same as for 3-bit BEC codes [23].

In this section, we discussed the error space satisfiability issue of the correctable errors. The number of check parity bits used for the proposed code should meet the requirement of (6). This restricts the check bit number and the minimum size of the dimension of H matrix. The issue of the column vector selection for the unique syndrome of a correctable error is discussed in Section III-B.

B. Unique Syndrome Satisfiability

From the view of binary block linear codes, if a type of error patterns can be corrected, the syndrome of individual error patterns should be unique. For the proposed code, the error patterns are (. . . , 1, . . .) for SEC, (. . . , 11, . . .) for DAEC, (. . . , 111, . . .) for TAEC, (. . . , 1111, . . .) for QAEC, and (. . . , 101, . . .) for 3-bit almost adjacent errors correction. Therefore, the unique syndrome satisfiability can be expressed by

$$S_{0i} \neq S_{0j}, \quad S_{1i} \neq S_{1j}, \quad S_{2i} \neq S_{2j} \quad (7)$$

$$S_{3i} \neq S_{3j}, \quad S_{4i} \neq S_{4j} \quad (8)$$

$$S_{0i} \neq S_{1j} \neq S_{2k} \neq S_{3l} \neq S_{4m} \quad (9)$$

where S0i is the syndrome for single bit error, S1i is the syndrome for double adjacent bit

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errors, S2i is the syndrome for triple adjacent bit errors, S3i is the syndrome for 3-bit almost adjacent bit errors, and S4i is the syndrome for quadruple adjacent bit errors. The syndrome variables S0i , S1i , S2i , S3i, and S4i are linear combinations of the H matrix columns obeying the rules in

$$S_{0i} = h_i \quad (10)$$
$$S_{1i} = h_i \oplus h_{i-1} \quad (11)$$
$$S_{2i} = h_i \oplus h_{i-1} \oplus h_{i-2} \quad (12)$$
$$S_{3i} = h_i \oplus h_{i-2} \quad (13)$$
$$S_{4i} = h_i \oplus h_{i-1} \oplus h_{i-2} \oplus h_{i-3} \quad (14)$$

where i , j ∈ [1, n], i ——————————— = j . Equations (10)–(14) indicate the detail relation between the syndromes and the columns. It is also used to design the circuits of syndrome calculation block. The code design is a kind of Boolean satisfiability problem. Normally, the solution of this problem is based on the recursive back tracing algorithm, which is presented in Section. Here, from the view of the integrated circuits design, two criteria are considered to optimize the target codes.

1) Smallest Hamming Weight of H: This criteria commonly indicates that the solution can be completed by using the lowest number of the logic gates in the synthesis process of the encoder and decoder.

2) Smallest Hamming Weight of the Heaviest Row of H: Logic depth in the encoding and decoding process depends on the logic path with the largest delay. The smallest hamming weight in the heaviest row can decrease the delay of the encoder and decoder.

With these restrictions discussed previously, based on the algorithm in Section IV, the solution for 3-bit BEC with QAEC codes can be found.

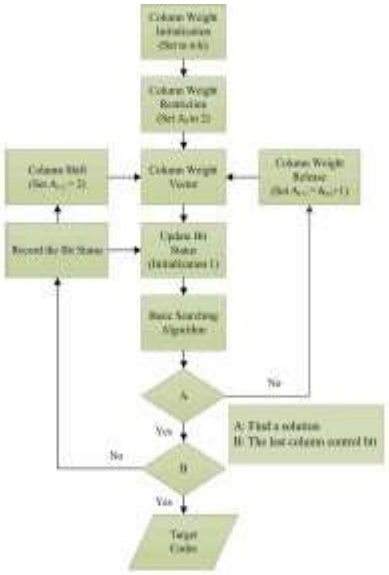

Fig. 5. Flow of algorithm with column weight restriction and past procedure record.

TABLE II
PERFORMANCE OF PROPOSED ALGORITHM FOR 3-bit BEC CODES

(n, k)	Smallest Total Ones		Smallest Heaviest Row	
	Codes [23]	Proposed Algorithm	Codes [23]	Proposed Algorithm
(23,16)	46(8)	45(7)	7(49)	7(45)
(40,32)	90(15)	88(13)	12(91)	12(89)
(73,64)	180(25)	180(21)	23(182)	21(180)

such as the one used in [23]. Therefore, they can be applied for the finding process of the

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QAEC codes. Normally, the solution of this problem is based on the recursive back tracing algorithm, which is presented in Section. The solutions found for QAEC codes are presented Section V.

PROPOSED CODES

In terms of computing time, it is possible for QAEC codes with 16 data bits to have access to all the solutions, but it is impossible for QAEC codes with 32 and 64 data bits. Therefore, in this paper, the best solutions are presented for QAEC codes with 16 data bits and the best solutions found in a reasonable time (one week) using the proposed searching algorithm are presented for QAEC codes with 32 and 64 data bits. In terms of the two optimization criteria mentioned in Section, for codes (23, 16), the two best parity check matrices are shown in Figs. 6 and 7 with both criteria best optimized. The parity check matrix for (40, 32) optimized to reduce the total number of ones is shown in Fig. 8 and the parity check matrices for (40, 32) optimized to reduce the maximum number of ones in a row is shown in Fig. 9. For codes (73, 64), the solutions obtained with both criteria better optimized are the same. The matrix is shown in Fig. 10.

PROCEDURE OF ENCODING AND DECODING FOR QAEC CODES

In this section, we elaborate on the encoding and decoding procedure of the proposed 3-bit BEC-QAEC codes. The fundamental theory of encoding and decoding were discussed in

Fig. 6. Best parity check matrix for the (23, 16) 3-bit burst with QAEC optimized to reduce the total number of ones and the maximum number of ones in a row.

Fig. 7. Best parity check matrix for the (23, 16) 3-bit burst with QAEC optimized to reduce the total number of ones and the maximum number of ones in a row.

Fig. 8. Parity check matrix for the (40, 32) 3-bit burst with QAEC optimized to reduce the total number of ones.

Fig. 9. Parity check matrix for the (40, 32) 3-bit burst with QAEC optimized to reduce the maximum number of ones in a row.

Fig. 10. Parity check matrix for the (73, 64) 3-bit burst with QAEC optimized to reduce the total number of ones and the maximum number of ones in a row.

Section. Here, an example for 16 data bits is illustrated in Fig. 11 with the H matrix used in Fig. 6. Based on the structure of the parity check matrix, the check bits are calculated by the corresponding data bits. The new encoded codeword, the combination of check bits and

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data bits is stored in the memory. When the particles hit the memory resulting in MBUs, the contents of affected memory cells are flipped. Here, to elaborate on the correction ability of QAEC codes, quadruple adjacent bits are flipped on D2, D3, D4, and D5. In the decoding process, the syndrome is calculated using the stored check bits and data bits and the structure of the parity check matrix.

Through the corresponding relationship between the syndrome and the XOR result of the columns mentioned in Section II, the flipped bits can be located. With the flipped bits inverted, the errors from the storage stage in the memory are effectively corrected. This is the whole procedure of encoding and decoding for the proposed QAEC codes.

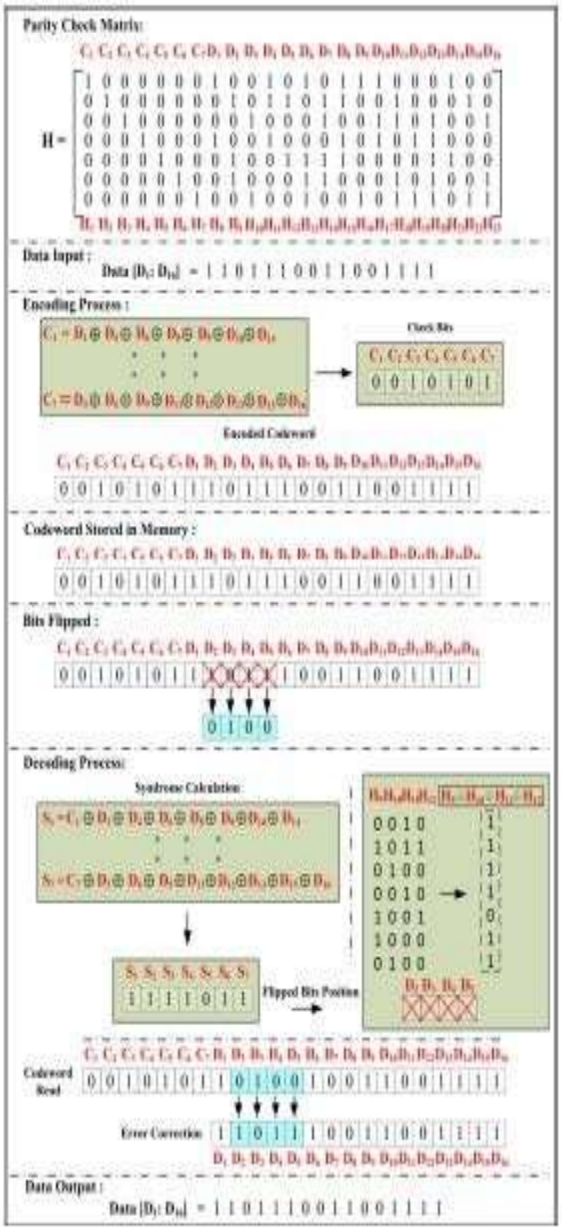

Fig. 11. Procedure of encoding and decoding for QAEC codes.

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RESULTS

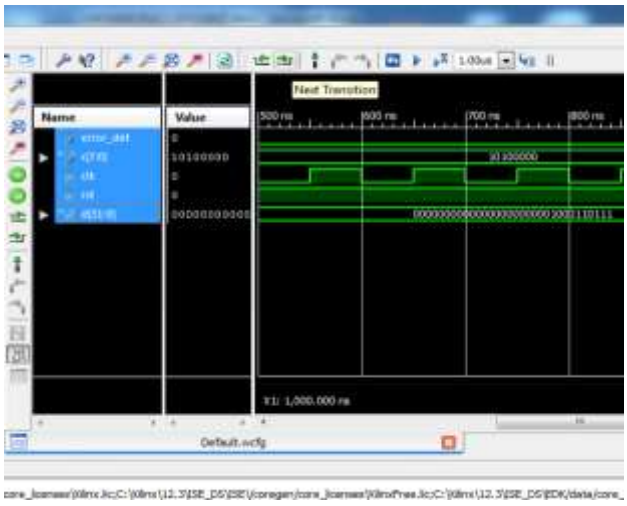

Fig1. Simulation output when clk is in state-0

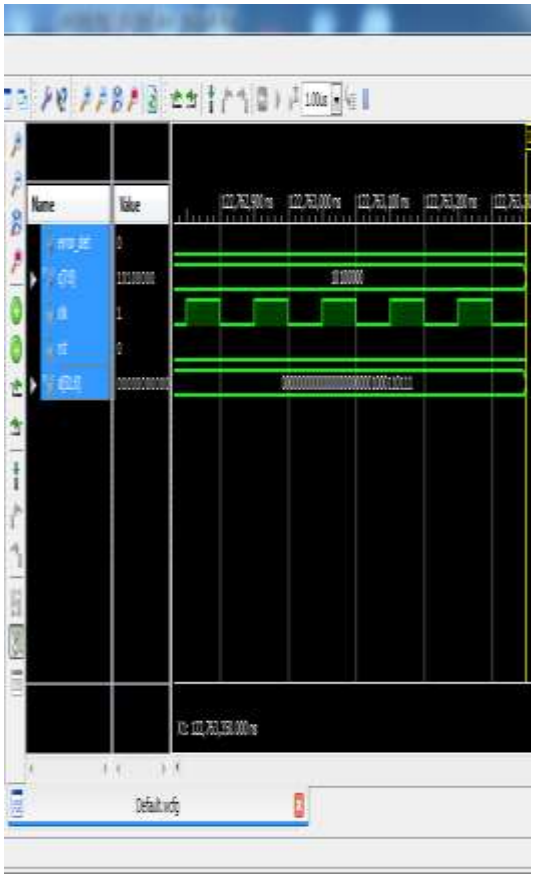

Fig.2. Simulation output when clk is in state-1

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	8	960	0%
Number of 4 input LUTs	16	1920	0%
Number of bonded IOBs	43	66	65%
Number of GCLKs	1	24	4%

Fig. Device utilization summary

```
Offset:          2.894ns (Levels of Logic = 2)
  Source:        rst (PAD)
  Destination:   m2/m1/c_0 (FF)
  Destination Clock: clk rising

  Data Path: rst to m2/m1/c_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            16    1.106   0.879  rst_IBUF (m2/m1/c_0_not0001)
     MUXF5:S->O            1    0.641   0.000  m2/m1/c_7_mux0001_f5 (m2/m1/c_7_mux0001)
     FDR:D                      0.268          m2/m1/c_7
    ----------------------------------------
    Total                      2.894ns (2.015ns logic, 0.879ns route)
                                       (69.6% logic, 30.4% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 9 / 9
--------------------------------------------------------------------------
Offset:          4.040ns (Levels of Logic = 1)
  Source:        m2/error_det (FF)
  Destination:   error_det (PAD)
  Source Clock:  clk rising

  Data Path: m2/error_det to error_det
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
```

Fig.3.Timing Summary

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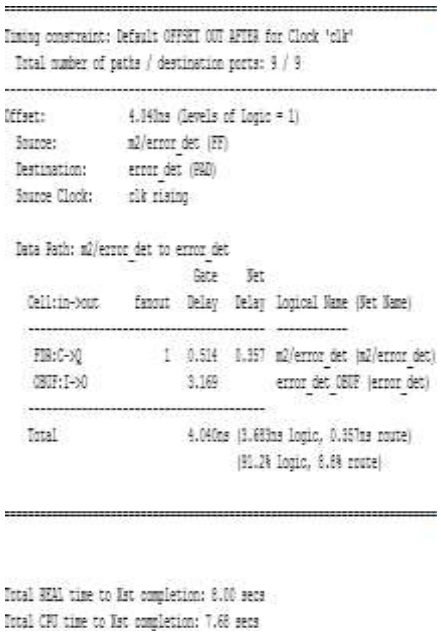

Fig.4.Timing constraints: Total Gate Delay

CONCLUSION

In this paper, a technique to extend the 3-bit BEC codes with the QAEC is presented. The proposed codes have the same redundancy as the previous 3-bit BEC codes [23]. To accelerate the searching process of target matrices, a new algorithm with column weight control and recording function is proposed. Based on the proposed algorithm, a searching tool is developed to execute the searching process automatically. To prove the validity of the proposed algorithm, it is applied to the previous 3-bit BEC codes [23] and the codes are remarkably improved on the two optimization criteria. Then, the proposed algorithm is used to find the solution for the QAEC. The complete solution searching process is finished for 16 data bits and the searching process using optimization algorithm is carried out for 32 and 64 data bits. Therefore, in this paper, the best solutions are presented for 16 data bits and the best solutions found in a reasonable computation time are presented for 32 and 64 data bits. The encoder and decoder of the proposed codes are implemented by using the HDL and synthesized for a 65-nm library. The overhead of area and delay is moderate versus previous 3-bit BEC codes [23]. This suggests that the proposed 3-bit BEC with QAEC codes can be effectively used by designers to protect the SRAM memories from radiation effect and mitigate the MBUs that affect up to four adjacent bits. Finally, as noted before, the proposed scheme could be extended to design 3-bit burst ECCs that can correct another of the 4-bit burst error patterns instead of the quadruple adjacent error. This can be of interest for applications in which there is a dominant 4-bit burst error pattern that is not the quadruple adjacent error.

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