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EFFICIENT COMBINATIONAL LOGIC CIRCUIT DESIGN USING QUANTUM- DOT CELLULAR AUTOMATA

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ABSTRACT:

Today's Technology era makes the devices as much as very thin and compact size as well as the minimum power consumption. To reduce the power consumption as well as increase the throughput, MOS device can be reduced by the device scaling technology. As per the technology's size shrink it couldn't be hold the Moore's law for next few years. This leads to force the thrust of new technology in emerging trends. For such a one of the new trends is the quantum logic and quantum cellular. Quantum Cellular Automata (QCA) provides a new approach in circuit design that technology promises extraordinary high computing speeds and low heat dissipation. QCA use the crossovers for optimization of circuits by reducing the cell count and area. The reduction in cells further leads to the reduction in the overall power dissipation. As this technology is in its primitive stage, many researchers are working towards to optimize the in this field. After a breakthrough in the physical implementation of the basic quantum cell the new technology is mainly focused on implementing digital design. Devices based on quantum mechanism is more fast and power efficient as it works in smallest physical form that is atomic level and only uses current in the range of nano amperes. Quantum cells are based on superposition and entanglement principle. The basic necessity of achieving low power consumption which the researchers in the field of VLSI are trying to accomplish with QCA technology. The Quantum cells based research is carried out in very broad area such as complex combinational circuit design. In our paper, a QCA based combinational circuit has been implemented and optimized the design in terms of area and power. The proposed design's circuit metric has been compared with the reference design model

1. INTRODUCTION

Today's semiconductor industry has been boon due to the advancement of the technology. This advancement methods leads to shrink the device size day by day that impact in the Very large scale . It was as early as 1965 when Gordon Moore predicted that the number of transistors can be integrated on to a single chip will double every 18 months. This law put forth by Moore has been a benchmark for semiconductor scaling for more than four decades. The IC industry which has been primarily driven by CMOS technology scaling is now forced to look into other alternatives as the scaling is fast approaching its fundamental limits. The International Technology roadmap for semiconductors (ITRS) has predicted that size limit of CMOS technology will be limited to about 5nm to 10nm and believes this limit is reached early. As the devices are exponentially scaled down various factors including power dissipation, gate leakage current, interconnection noise and stray capacitances are tha potential bottleneck that leads to the degradation of circuit performance. The increasing prominence of portable systems and the need to limit power consumption in very density VLSI chips have lead to rapid and innovative developments in low power design during the recent years. The driving forces behind these developments are portable applications requiring low power dissipation and high throughput, such as notebook computers, portable communication devices and personal digital assistants.

The need for low power design is also becoming a major issue in high- performance systems such as microprocessors and digital signal processors and other applications. Increasing chip density and high operating speed lead to the design of very complex chips with high clock frequencies. If the clock frequency of the chip increases then the power dissipation of the chip, and the temperature increases rapidly[12].

Quantum-Dot cellular Automata (QCA) is currently being investigated as an alternative to CMOS technology. There has been extensive study on a wide range of circuits from simple logical circuits such as adders to complex circuits, 4-bit processors. At the same time, little if any work has been done in considering the possibility of reconfiguration to reduce power in QCA devices. This work presents the such efforts when considering reconfigurable QCA architectures which are expected to be both robust and power efficient. We present a new reconfiguration scheme which is highly robust and is expected to dissipate less power with respect to conventional designs.

QCA is one such nano computing paradigm that exploits some of the unavoidable nanoscale issues such as quantum effects and device integration for performing useful computation. Some of the potential advantages of QCA include the lack of interconnects, high clock frequency and since QCA doesn't involve transfer of electrons or flow of current, it has the potential to perform low power computing. One of the most striking features of this emerging technology is that it has the ability to dynamically reconfigure or redesign the functionality of the system which makes the system more powerful and more efficient in terms of computational speed and power dissipation.

QCA can be exploited to design various low power circuits which are not efficient in terms of power but are also efficient in terms of area and computation. In QCA that is based on the change in polarization of electrons in a QCA cell. In this QCA a new custom wire crossing technique which is used to overcome the traditional problems of routing in any reconfiguration based design. The design exploits the inherit pipeline nature of QCA which can lead to an enormous reduction in area since the entire computation can be computed in a single block. One can design highly energy efficient circuits as QCA doesn't involve the physical movement of any charge particles. This design will be highly energy efficient along with added advantages of pipelining and area.

2. LITERATURE SURVEY

Aishwarya Tambe, SnehalBharke, SankitKassa [1,2,3] published a inrternational journal innovative technology and exploring engineering(IJITEE) is design and analysis of (2*1) and (4*1) multiplexer circuit in quantum dot cellular automata approach. The proposed Multiplexer is compared with previous designs. Multiplexers are required in many coherent and functional circuits. This paper represents an innovative design of a multiplexer in QCA. The construction of the proposed 2:1 MUX is simple, it is composed of rotating two 2-input AND, using a common polarized QCA cell and a two-input OR gate. The main focus of this implementation is to reduce circuit complexity and increase efficiency. Theproposed designs are efficient in terms of overall area and cell count. The proposed design saves upto 63.15% number of QCA cells and 66% of area compared to previous design approaches. This circuit can also portray a crucial role in the area of digitalnano communication for signals encoding in near future.

A.Mallaiah, G.N.Swamy, K. Padmapriya[4,5] published a international journal of scientific & Engineering research is designing efficient multiplexer demultiplexer QCA logic circuits and power dissipation analysis – A new approach. The proposed 2*1 mux configuration involves just 0.04 micro m^2 region compared to previous one. The main focus of this implementation is to reduce circuit complexity and increase efficiency. The proposed design saves upto 66.6% and 57.14% of area compared to previous design approaches. The proposed configuration has been examined and utilized QCA software. At long last the outcomes guarantee the predominance of over earlier outlines as far as area, cell count and power dissipation.

Firdous Ahmad[6] published an optimum designof QCA based 2^n:1/1:2^n multiplexer/demultiplexer and its efficient digital logic realization. The construction of the proposed 2:1 MUX is simple, it is composed of rotating two 2-input AND, using a common polarized QCA cell and a two-input OR gate. The main focus of this implementation is to reduce circuit complexity and increase efficiency. This paper presents novel approach to implement 2:1 MUX and 1:2 DEMUX circuits using 2 electrons 4 dot QCA. The proposed 2:1 MUX has been used to implement basic digital logic elementary for QCA. Any higher order MUX/DEMUX can be implemented using the proposed 2:1MUX and 1:2 DEMUX respectively. Therefore, using the proposed 2:1 MUX and 1:2 DEMUX an efficient 4:1 MUX and 1:4 DEMUX have been proposed. Power dissipation analysis of the designed 2:1 MUX has been done which is proclaiming fact that the designed 2:1 MUX is power efficient than other conventional counterparts. The proposed design has shown significant improvements in comparison to previously designed multiplexers in terms of area and complexity.

SohankumarDahana, Aastha Hajari[7,8] published a International journal of Trend in Scientific Research and Devolopment is Efficient design of 2:1 MUX using nanotechnology based on QCA. In this paper they explained multiplexer is a combinational logic component that has several inputs and only one output. Mux directs one of the inputs to its output line by using a control bit word to its select line. A multiplexer can take anynumber of input line but than the selection line will be according to the number of inputs. The mux are important part of digital logic circuits and control systems. In this paper, proposed designs for QCA 2:1mux were reviewed. The functionality of the proposed circuits is necessary to validate the designs using the QCA designer. The proposed design, in terms of cells as better operation compare to the other existing some designs.

Reena Singh Ahirwah,Jyoti Dixit, Kavitha Singh Bagla, Umesh Barahdia [9,10,11] design adequate multiplexer using quantum-dot cellular automata. Literature review of this paper is based on various arrangenments of the QCA cells wide spread range of QCA multiplexer designs have been reported. This pap er presents novel approach to implement This paper presents novel approach to implement 2:1 MUX and 1:2 DEMUX circuits using 2 electrons 4 dot QCA. The proposed 2:1 MUX has been used to implement basic digital logic elementary for QCA. Any higher order MUX/DEMUX can be implemented using the proposed 2:1 MUX and 1:2 DEMUX respectively. Therefore, using the proposed 2:1 MUX and 1:2 DEMUX an efficient 4:1 MUX and 1:4 DEMUX have been proposed. Power dissipation analysis of the designed 2:1 MUX has been done which is proclaiming fact that the designed 2:1 MUX is power efficient than other conventional counterparts. The proposed design has shown significant improvements in comparison to previously designed multiplexers in terms of area and complexity.

M.Kianpour', R.Sabbaghi-Nadooshan [12,13] published a optimized design of multiplexer by quantum-dot cellular automata in this paper 2:1 multiplexer is used as module to implement the 2^n:1 multiplexer in this paper they present successful simulation of the 2:1,4:1 multiplexer with QCA design. They presented a new design of 2:1 multiplexer in the QCA, which could achieve a high efficiency. In each section we explained the application of 2:1 multiplexer in designing and implementing 4:1 and 8:1 multiplexers. The 2:1 multiplexer presented in this paper, with three majority gates has been implemented, which we used as two- input AND gate and OR gate with fixed one of inputs. In general, an electronic multiplexer allows a system to select one of the several input signal and forward it to the output. The modularity of the design method allows the determination of the number of QCA cells and the covered area for the 2^n:1 QCA multiplexers compared to previous works significantly improved area, complexity, delays and power consumption. These multiplexers can be used in processors with high operating speed and this circuit is applicable in the core of high-speed FPGA and ALU processors.

Sara ashemi, Mostafa Rahimi Azghadi, Ali ZakerolHosseni [14,15,16] published a novel QCA multiplexer design. Multiplexers are important components and they re used in many logical and functional circuits. This paper presents a novel design of a 2:1 multiplexer in QCA. In addition we can construct larger multiplexers (8:1, 16:1 and etc) based on our 2:1 multiplexer design. It is inferable from simulation results that the proposed multiplexer achieved significant improvements in QCA circuits as compared to previous common designs. The proposed structures lead to denser construction and consequently more efficient QCA circuits. Besides these improvements, one of the main contributions in this paper is designing robust QCA multiplexer as it is reliable in high input frequency where its counterparts do not act properly. This proposed multiplexer saves upto 55% of count and 51% of area.

3. PROPOSED WORK

3.1 Basic Elements

Quantum-dot Cellular Automata (QCA) is a new nano computing paradigm which encodes binary information by charge configuration within a cell instead of the conventional current switches. There is no current flow within the cells since the coulombic interaction between the electrons is sufficient for computation. This paradigm provides one of many possible solutions for transistor-less computation at the nanoscale.

QCA cell

The standard QCA cells have four quantum dots and two electrons. There are various kinds of QCA cells proposed which include a six-dot QCA cell and an eight-dot QCA cell. In a QCA cell, two electrons occupy diagonally opposite dots in the cell due to mutual repulsion of like charges. An example of a simple unpolarized QCA cell consisting of four quantum dots arranged in a square is shown in fig.

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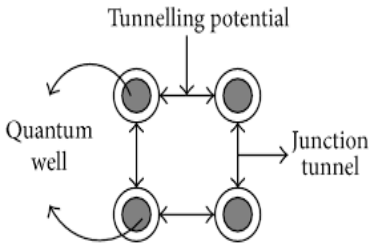


Figure 1 : QCA cell

The information in QCA cells is transferred due to coulombic interactions between the neighbouring QCA cells, the state of one cell influences the state of the other. The basic logic devices in QCA are:

Binary Wire

A binary wire can be viewed as a horizontal series of cells to transmit information from one cell to another. It is typically divided into various clock zones, to ensure that the signal doesn't deteriorate as signals generally tend to degrade with a long chain of cells in the same clocking zone.

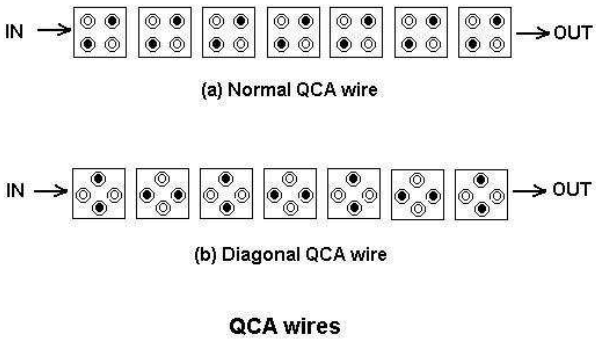
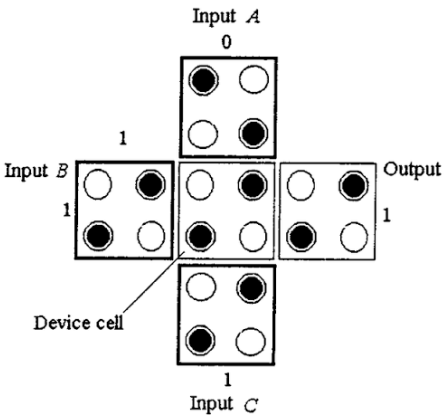


Figure 2: QCA wire

Majority Gate

Majority gate is the fundamental logic block in any QCA design. A majority gate can be built with the help of five cells. The top, left and bottom cells are inputs. The device cell in the center interacts with the three inputs and its result will be propagated to the cell on the right. An example of an majority gate representation in QCA is as shown in fig



Truth table

A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

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Figure 3: Majority gate and its truth table

$$F(A,B,C) = A.B + B.C + C.A$$

A majority gate is the basic logic gate in QCA, as it can function as on OR gate with one of the inputs fixed to 1 and function as an AND gate with one of the inputs fixed to 0.

3.2 Proposed EXOR gate

The XOR is a logic operation on two operands that results in a logical value of true if and only if one of the operands, but not the true, has a value of true. This forms a fundamental logic gate in many operations to follow.

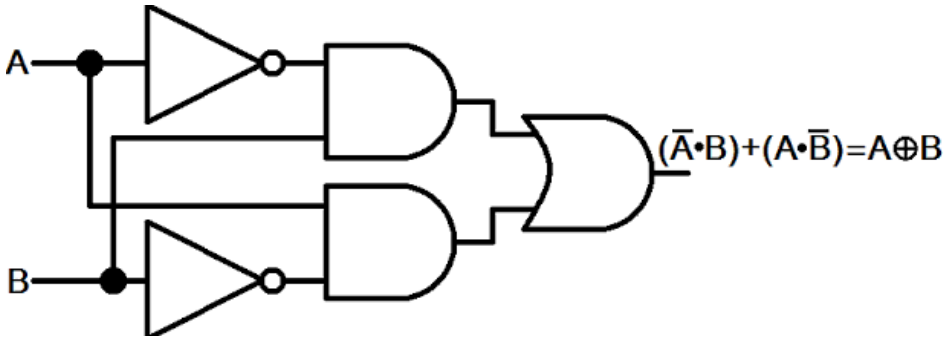

Figure 4: XOR gate

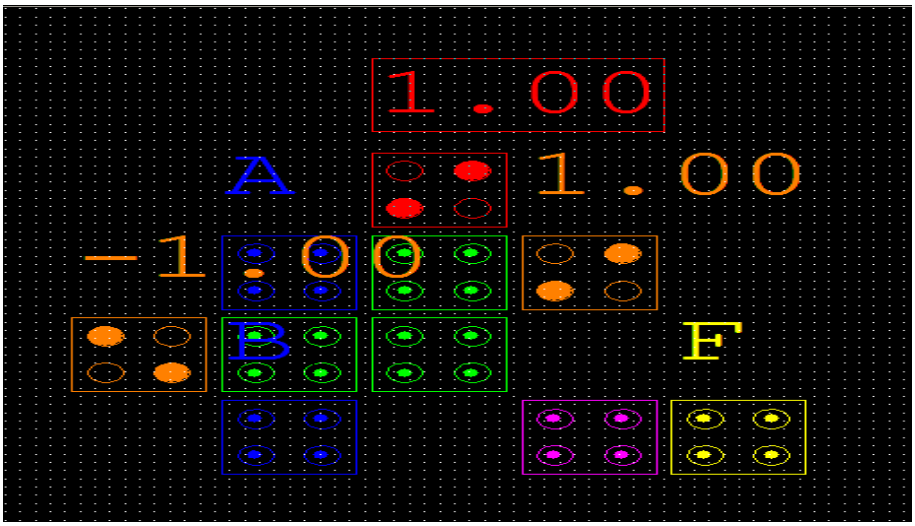

Figure 5: The layout of EXOR gate

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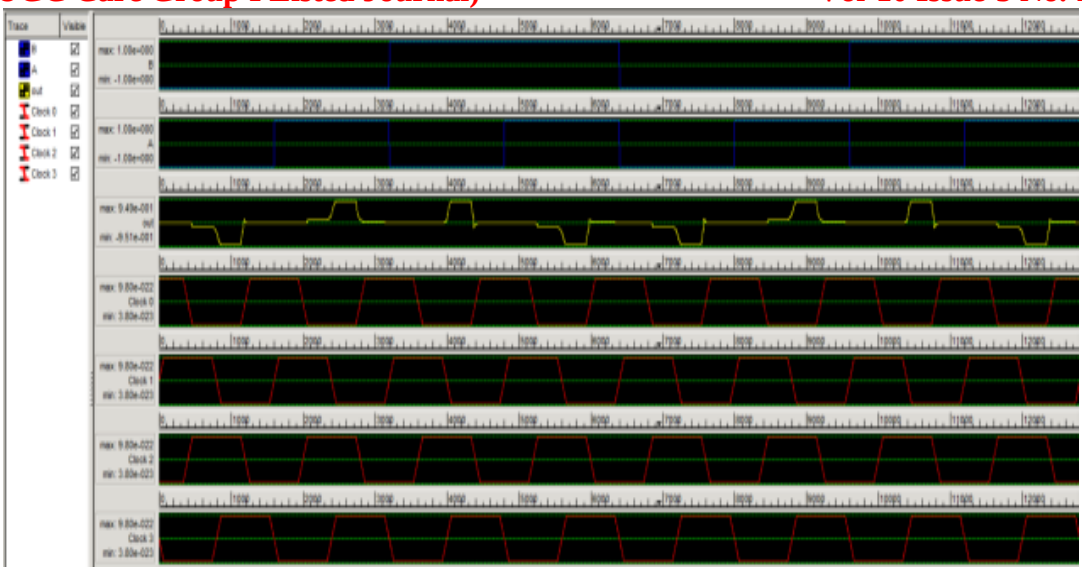

Figure 6: Simulation output of EXOR gate

3.3 Proposed 2:1 MUX

Multiplexer have aconsiderable role in the digital systems which allow us to select one of the inputs flows for transmitting to the output. The 2:1 multiplexer presented in this paper, with three majority gates has been implemented, which we used as two- input AND gate and OR gate with fixed one of inputs.

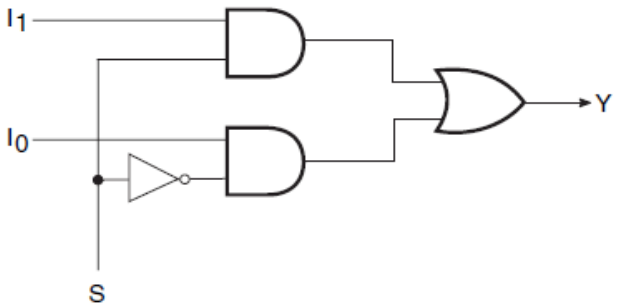

Figure 7: Logic diagram of 2:1 MUX

The 2:1 multiplexer in the first component uses two 2-input AND gates. The inputs of AND gates are connected to the selector wires, and the inputs I0 and I1lines through inverter gates needed as shown in fig above.

The second component uses one 2-input OR gates.

In QCA technology, each logic gate with more than three inputs is built by cascading multiple 3-input gates. The logic functionality is as follows: if the S rails are “0 or 1”, the outputs are setting with I0 or 11.

S	Y
0	I_0
1	I_1

3.4 IMPLEMENTATION OF 2:1 MULTIPLEXER IN QCA

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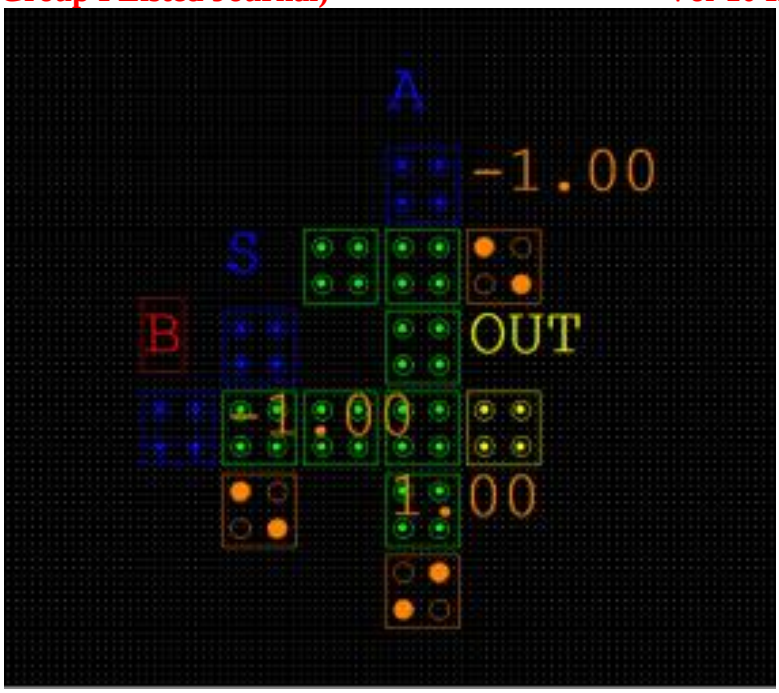

Figure 8: QCA layout of 2:1 MUX

The circuit is designed and simulated for functional behavior using the QCA designer version 2.0. the proposed 2:1 multiplexer consists of 14 cells covering an area of 0.02micrometer^2.

4. RESULT AND DISCUSSION

The simulation results of the 2:1 multiplexer are presented in below fig.

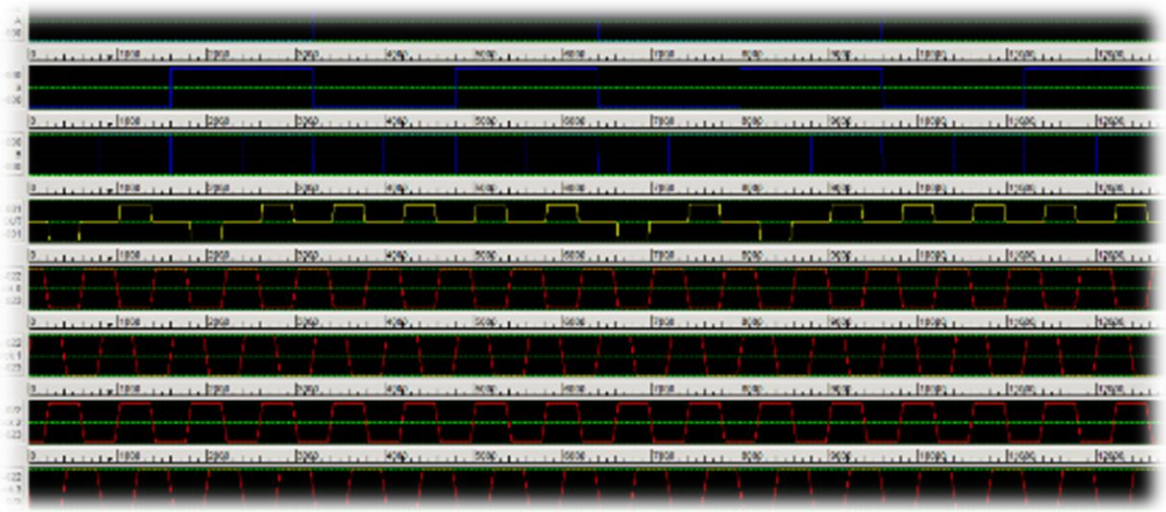

Figure 9: Simulation output of 2:1 MUX

The performance table for 2:1 MUX

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2:1 Multiplexer	Cell Count	Area (μm^2)	Latency (clock cycle)	Energy Dissipation (eV)
[3]	23	0.04	2	**0.0137**
[1]	19	0.02	3	**0.0151**
[4]	18	0.017	2	**0.0133**
[5]	17	0.0217	2	**0.0133**
Proposed	**14**	**0.0105**	**2**	**0.00902**

5. CONCLUSION:

The designs proposed are designed using efficient design methodology where a 2:1 Multiplexer is used as a building block. The proposed 2:1 multiplexer is optimized and the cell count is reduced by 18 %, area is reduced by 49% and the energy dissipation is reduced by 32% when compared with the design in [5]. The proposed designs of 2:1 Multiplexer and XOR gate along with Shift register can be used to implement a compact pseudo random number generator.

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