ISSN: 2278-4632
Vol-10 Issue-12 No.03 December 2020

Implementation of Efficient Multi Bit Adder Using GDI Based Hybrid Digital Circuits

B.V. Aravind[1], N. Naveen Kumar[2], G. Aruna Kumari[3]
[1]Assistant Professor, [2]Assistant Professor, [3]Assistant Professor, ECE Department, Anantha Lakshmi Institute of Technology and Sciences, Ananthapuramu, Andhra Pradesh, India.

ABSTRACT: The rapid advance in multimedia and digital communication systems, real time signal processing like audio signal processing, image and video processing. The aim of this work is to design 1-bit full adder circuit using full-swing GDI to reduce power consumption, delay and area, in addition to achieve full-swing output. This paper presents a design which provides full swing output for logic 1 and logic 0 for 1-bit full adder cell and reduces power consumption, delay, and area. In this design full adder consists of two XOR gate cells and one cell of 2x1 multiplexer (MUX). The performance of the proposed design compared with the different logic style for full adders. Implementing a 4-bit ripple-carry adder using GDI based hybrid adder.

1.INTRODUCTION

Adder is one of the significant building blocks in the construction of a binary multiplication. In recent times, applications are aimed at battery operated devices so that power dissipation becomes one of the primary design constraints. In the past processor speed, circuit speed, area, performance, cost and reliability were of prime importance. Power consumption was of secondary concern. However, in recent years power consumption is being given equal importance. The reason for such a changing trend is attributed probably due to the rapid increase in portable computing devices and wireless communication systems which demand high speed computations and complex functionality with low power consumption. In addition to this high performance processors consume severe power which in turn increases the cost associated with packaging and cooling. Subsequently there is a rise in the power density of VLSI chips thereby disturbing the reliability. It has been found that every 10o rise in operating temperature roughly doubles the failure rate of components made up of Silicon due to several Silicon failure mechanisms such as thermal runaway, junction diffusion, electro migration diffusion, electrical parameter shift package related failure and Silicon interconnect

ISSN: 2278-4632
Vol-10 Issue-12 No.03 December 2020

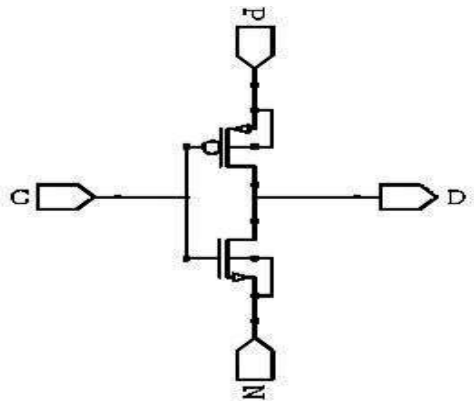
failure. From the environment point of view, the lesser the power dissipation of electronic components, lesser will be the heat dissipated in rooms which in turn will have a positive impact on the global environment. Also, lesser electricity will be consumed. Therefore, for further optimization of performance of a full adder in terms of power consumption, delay time as well as Power Delay Product (PDP), a new low power, high speed energy efficient full adder is being proposed using Gate Diffusion Input (GDI) technique. GDI is a novel modus operandi for low power digital circuits. This procedure allows reduction in power consumption, propagation delay and transistor count of digital circuit. The method can be used to minimize the number of transistors compared to conventional Complementary Pass-transistor Logic (CPL) and Dual Pass transistor Logic (DPL) CMOS design. The proposed adder has a transistor count of 14— a reduction of 72.00%, 63.16% and 58.82% compared to a full adder composed of CMOS logic, transmission gates and CPL, proposing a reduction in area. In order to establish the technology independent design , this adder is proposed..

2. EXISTING METHOD

The GDI technique offers realization of extensive variety of logic functions using simple two transistor based circuit arrangement. This scheme is appropriate for fast and low-power circuit design, which reduces number of MOS transistors as compared to CMOS and other existing low power techniques, while the logic level swing and static power dissipation improves. It also allows easy top- down approach by means of small cell library [5]. The basic cell of GDI is shown in Fig. 2.

1) The GDI cell consists of one nMOS and one pMOS. The structure looks like a CMOS inverter. Though in case of GDI both the sources and corresponding substrate terminals of transistors are not connected with supply and it can be randomly biased.

2) It has three input terminals: G (nMOS and pMOS shorted gate input), P (pMOS source input), and N (nMOS source input). The output is taken from D (nMOS and pMOS shorted drain terminal) [11].



ISSN: 2278-4632
Vol-10 Issue-12 No.03 December 2020

Fig 1 GDI basic cell consisting of pMOS and nMOS

GDI logic style approach consumes less silicon area compared to other logic styles as it consists of less transistor count. In view of the fact that, the area is less, the value of node capacitances will be less and for this reason GDI gates have faster operation which presents that GDI logic style is a power efficient method of design.

We can realize different Boolean functions with GDI basic cell. Table I shows how different Boolean functions can be realized by using different input arrangements of the GDI cell.

N	P	G	Out	Function
'0'	B	A	$\bar{A}B$	F1
B	'1'	A	$\bar{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
'0'	'1'	A	$\bar{A}$	NOT

Table I. Truth Table Of GDI Cell

3. ARCHITECTURE OF EXISTING GDI FULL ADDER

The proposed system designs full adder circuit using Gate diffusion Input (GDI) technique. Using this technique one can design a digital circuit with low power in embedded system. The number of transistors used in the circuit is minimum hence they are used by the circuit is reduced as well as the delay and power consumption.

Full adder is a combinational circuit that performs the arithmetic operation of 3 number of bits. Addition considered an essential operation in arithmetic and logic unit digital signal processing and. The 1-bit full adder contains three input bits and two output bits, the first two bits of the inputs are A and B called operands and the third input bit Cin is a bit carried in from the previous less-significant stage, output bits called sum is the result of addition operation and carry out which will be the input carry to the next addition operation, and the expression:

$$SUM = A \oplus B \oplus Cin$$

$$COUT = A\,\overline{(A \oplus B)} + Cin\,(A \oplus B)$$

The proposed design consists of 16 transistors including two XOR gate cells to produce sum and one multiplexer cell to produce carry out, as shown in figure (2), the block diagram shown in figure (3), and the truth table of proposed full adder presented in table II

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

ISSN: 2278-4632
Vol-10 Issue-12 No.03 December 2020

Table II. Truth Table Of Proposed Full Adder

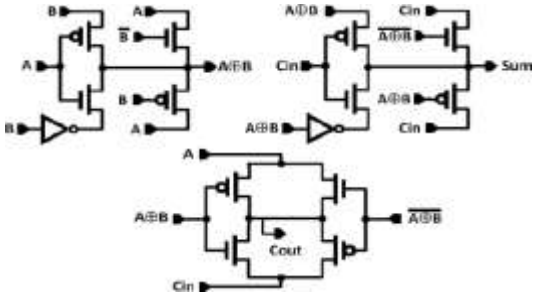


Fig.2. Proposed design for 1-Bit Full Adder

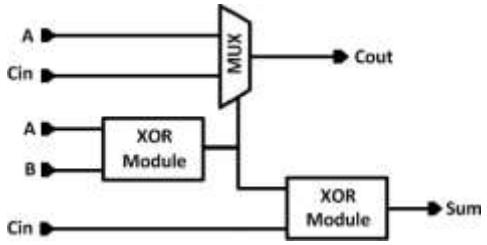


Fig. 3. Block Diagram For Proposed Full Adder

The major benefit of using GDI technique is that a large number of functions can be implemented using this technique. We can see from the table 2 that GDI can be used for implementing various designs such as MUX, AND, OR etc. The most complex design among these is the designing of MUX, which can be done using 2 transistors. Whereas using other conventional techniques it requires 8-10 transistors for designing a MUX. The main drawback of GDI technique is that of swing degradation. This is due to threshold loss and to eliminate this we have to use silicon on insulator or twin-well process to realize, which is very expensive. Designing a full adder the major building block is XOR gate using GDI technique.

4. PROPOSED METHOD

The design of a new energy efficient hybrid full adder implemented using the MVT-GDI approach. As per implementation operating the circuit at ULV, the transistors will be in subthreshold/ weak-inversion region, and the sub-threshold current of a MOS device is given by the (1) .

$$I\text{Sub} = I0e\ Vgs - VT\ /nV\text{th} \quad (1)$$

where $I0$ is the drain current when $Vgs = VT$ and is given by

$$I_0 = \mu_0 C_{ox} \frac{W}{L}(n-1)V_{th}^2 \quad (2)$$

The parameters VT is the threshold voltage, Vgs is the gate to source voltage, n is the sub-threshold slope factor ($n = 1 + Cd\ /Cox$) and Vth is the thermal voltage (kT/q) of the transistor. From (1), it can be understood that there will be a significant degradation in the performance of the sub-threshold CMOS logic circuits due to the exponential increase in the delay. Although, it was shown that the sub-threshold and gate leakage components for GDI cell are significantly less, compared to a static CMOS gate but there will be a

ISSN: 2278-4632
Vol-10 Issue-12 No.03 December 2020

significant impact on the performance of the GDI circuits because of the poor logic swing caused by the *VT* drop. In order to reduce this impact, the transistors in the critical path which has threshold drop are replaced with low *VT* transistors in the proposed design. However, the use high *VT* devices in non-critical paths can reduce the power consumption, but at ULVs, it may lead to functionality failure of the design. So, the authors did not prefer using high *VT* cells in the proposed designs in order to improve the performance which is very critical in sub-threshold operation for minimizing the energy consumption. Transistor sizing also plays a key role in deciding the performance of the design. Initially, the sizing of the transistors is done based on the theoretical background of the full adder circuit design and the CMOS the previously set values to obtain the best performance in terms of energy consumption through the simulations.

The functionality and the structure of the proposed adder design is explained as follows.

Proposed hybrid full adder design

In general, the logic functions of a basic 1-bit full adder can be represented as in (3) and (4)

$$\text{Sum} = (\text{A} \oplus \text{B}) \oplus C_{\text{in}} \quad (3)$$

$$C_{\text{out}} = (\text{A} \cdot \text{B}) + C_{\text{in}} \cdot (\text{A} \oplus \text{B}) \quad (4)$$

The proposed full adder design employs only 14 transistors as shown in Fig.2. It mainly consists of five logic blocks designed using MVT-GDI technique. One XOR/XNOR, two multiplexer's, one Swing Restored Transmission Gate (SRTG), and the other one is Swing Restored Pass Transistor (SRPT) block. The XOR/XNOR block is designed using GDI technique. Since the path of the inverters used in the XOR/XNOR blocks has no voltage drop, they are incorporated with standard *VT* devices. Since the GDI MUX-1, multiplexes the output of the XOR (A AXOR B) and the XNOR (AXNOR B) with a control input (*C*in) to obtain the sum function. Therefore, the (3) can also be represented as in (5).

$$\text{Sum} = \overline{C_{\text{in}}}(\text{A} \oplus \text{B}) + C_{\text{in}}(\text{A} \odot \text{B}) \quad (5)$$

The carry output (*C*out) is generated by the GDI MUX-2, which multiplexes the inputs *C*in and B with control line from the output of XNOR logic (A XNOR B). Therefore, the (4) can also be represented as in (6).

ISSN: 2278-4632
Vol-10 Issue-12 No.03 December 2020

$$C_{out} = (\overline{A \odot B})C_{in} + (A \odot B)B$$

6

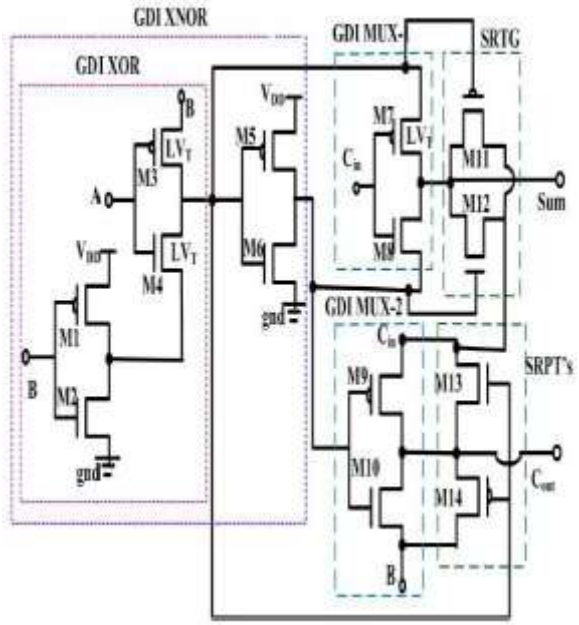


Fig. 4Proposed 14T MVT-GDI hybrid full adder design

However, the proposed structure looks similar to many previous XOR/XNOR logic-based designs and authors' previous GDI-based design, but none of the previous designs provides full logic swing with only 14 transistors. In the proposed design, the full swing is ensured using a SRTG at the output of the sum and SRPT's at the carry output (*C*out). It can be observed that the swing restoration transistors (M11, M12,M13, M14) are 'ON' when there is a *VT* drop at the output of the sum generation GDI MUX1 and *C*out generation GDI MUX-2 to provide full swing logic. Since there is no *VT* drop at the output in most of the cases as stated in Table 4, the transistors (M11, M12, M13, M14) are also incorporated with standard *VT* transistors

5. RIPPLE CARRY ADDER

Ripple-Carry Adders (RCA): The simplest way of doing binary addition is to connect the carry-out from the previous bit to the next bit's carry-in. Each bit takes carry-in as one of the inputs and outputs sum and carry-out bit and hence the name ripple-carry adder. This type of adders is built by cascading 1-bit full adders. A 4-bit ripple-carry adder is shown in Figure 2.3. Each trapezoidal symbol represents a single-bit full adder. At the top of the figure, the carry is rippled through the adder from cin to cout .It can be observed in Figure 3.1 that the critical path, highlighted with a solid line, is from the least significant bit (LSB) of the input (a0 or b0) to the most significant bit (MSB) of sum (sn-1).The ripple carry adder is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage.

The design of the 4-bit adder, based on the 1-bit adder, is almost trivial. As stated

ISSN: 2278-4632
Vol-10 Issue-12 No.03 December 2020

previously, all we need to do is duplicate the 1-bit adder four times, and connect each carry-out to the carry-in of the next adder in the series. This design scheme is presented graphically in Figure 5.This method for constructing a multi-bit adder is perfectly extendable, so much so that it would not be challenging to design even a full 64-bit adder. Again, however, breadboard space is at a premium, especially when working with bulky discrete components, so I will only be building a 4-bit adder.

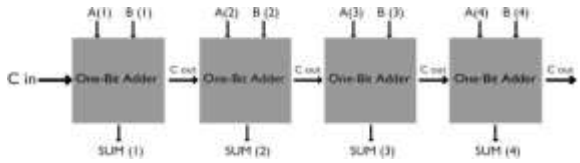


Fig 5: A graphical representation of the 4-bit adder with ripple carry.

5. RESULTS

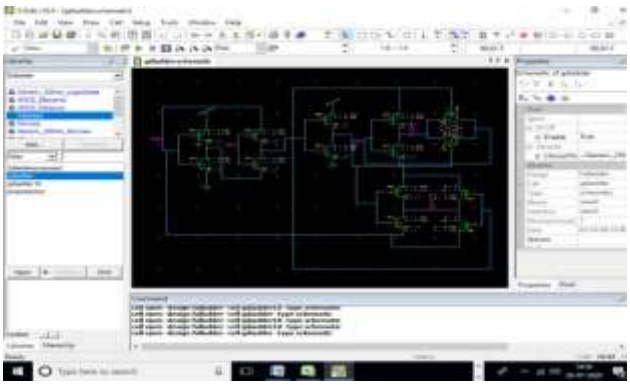


Fig 6 Circuit Diagram of proposed System

Fig 7 Simulation Result of Proposed System

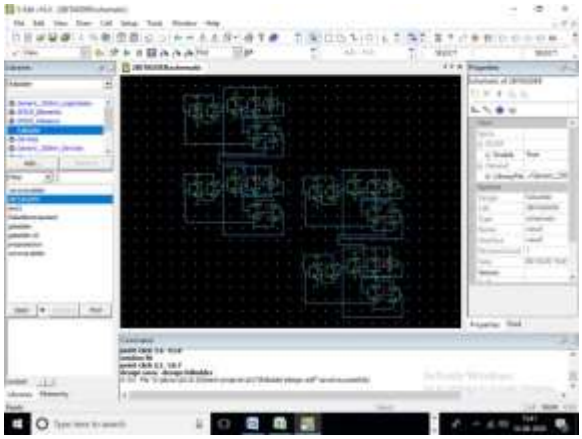


Fig 8 Circuit Diagram of four bit RCA adder

6. COMPRESSION TABLE

S.no		Existing System	Proposed System
1	Area(Transistor)	10	10
2	power	$9.92*10^{-7}$	$3.43*10^{-8}$

7. CONCLUSION

The goal of this paper was to design a full adder with high speed performance using GDI technique. From the performance analysis table it is clear that the proposed

ISSN: 2278-4632
Vol-10 Issue-12 No.03 December 2020

design system is the best among the discussed designs in terms of area, delay and power dissipation. Since the results were obtained as an outcome of simulation, the readings are precise. This design will have an improved speed and also the efficiency of the system is more compared to all the conventional techniques. Further modifications can be made in the design by adding a few more transistors.

REFERENCES

[1] Tripti Sharma, K.G.Sharma and B.P.Singh,"High Performance Full Adder Cell: A Comparative Analysis",2010 IEEE Students' Technology Symposium 3-4 April 2010,IIT Kharagpur, 2010.

[2] Rajkumar Sarma1 and Veerati Raju," Design and Performance Analysis of Hybrid Adders For High Speed Arithmetic Circuit", International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.3, June 2012.

[3] A. Morgenshtein, A. Fish, and I. Wagner, “Gate-diffusion input (GDI): a power-efficient method for digital combinatorial circuits,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems IEEE Trans. VLSI Syst., vol. 10, no. 5, pp. 566–581, 2002.

[4] A. Morgenshtein, I. Shwartz, and A. Fish, “Gate Diffusion Input (GDI) logic in standard CMOS Nanoscale process,” 2010 IEEE 26th Convention of Electrical and Electronics Engineers in Israel, 2010.

[5] A. Morgenshtein, V. Yuzhaninov, A. Kovshilovsky, and A. Fish, "Fullswing gate diffusion input logic—Case-study of low-power CLA adder design," Integration, the VLSI Journal, vol. 47, no. 1, pp. 62–70, Jan. 2014.

[6] Korraravikumar, AL Reddy, M.Sadanandam, Santhoshkumar.A and M.Raju," Design of 2T XOR Gate Based Full Adder Using GDI Technique", International Conference on Innovative Mechanisms for Industry Applications (ICIMIA 2017),2017.

[7] Jaume Segura, Charles F. Hawkins CMOS electronics: how it works, how it fails, Wiley-IEEE, 2004, page 132

[8] Clive Maxfield Bebop to the Boolean boogie: an unconventional guide to electronics Newnes, 2008, pp. 423-426

[9] Albert Raj/Latha VLSI Design PHI Learning Pvt. Ltd. pp. 150-153

[10] Yano, K, et al, "A 3.8 ns CMOS 16*16b multiplier using complementary pass transistor logic", IEEE J. Solid State Circuits, Vol 25, p388-395, April 1990

[11] Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha, and Jin-Gyun Chung, “A Novel Multiplexer-Based

ISSN: 2278-4632
Vol-10 Issue-12 No.03 December 2020

Low-Power Full Adder" IEEE Transaction on circuits and systems-II: Express Brief, Vol. 51, No. 7,p-345, July- 2004

[12] Makoto Suzuki, et al, "A 1.5 ns 32 b CMOS ALU in double pass transistor logic", ISSCC Dig. Tech. Papers, pp 90-91, February 1993.

[13] N. Ohkubo, et al, "A 4.4 ns CMOS 54X54 b multiplier using pass transistor multiplexer", Proceedings of the IEEE 1994 Custom Integrated Circuit Conference, May 1-4 1994, p599-602, San Diego, California.

[14] Mohamed W. Allam, "New Methodologies for Low-Power High-Performance Digital VLSI Design", PhD. Thesis, University of Waterloo, Ontario, Canada, 2000

[15] A.Bazzazi and B. Eskafi, "Design and Implementation of Full Adder Cell with the GDI Technique Based on 0.18µm CMOS Technology", International MultiConference of Engineers and Computer Scientists (IMES) Vol II, March 17 - 19, 2010, Hong Kong.