DESIGN OF LOW POWER DYNAMIC COMPARATOR FOR ANALOG TO DIGITAL CONVERTER

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Abstract:
The need for ultra-low-power, area efficient, and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this project, a low power double tail comparator is proposed. Based on the presented analysis, where the circuit of a conventional double-tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time and by using sleep transistor technique the power consumption is to be reduced. Simulation results in a 45nm CMOS technology confirm the analysis results. It is shown that in the proposed comparator both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 500MHz at supply voltages of 1V with power consumption 36.56nW.

Introduction

Due to the high demand of ultra-low power in digital application, the needs of energy efficient Analog-to-digital converter (ADC) are really essential. The comparator being an important part of Analog-to-digital converter needs to have optimum performance under low power condition.
Comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many high speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. High-speed comparators in ultra-deep sub-micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs.
Many techniques, such as supply boosting methods techniques employing body-driven transistors current-mode design and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. Boosting and bootstrapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but
They introduce reliability issues especially in UDSM CMOS technologies. Body-driven technique adopted by Blalock removes the threshold voltage requirement such that body driven MOSFET operates as a depletion-type device. Based on this approach, in a 1-bit quantizer for sub-1V modulators is proposed. Despite the advantages, the bod ydriven transistor suffers from smaller transconductance (equal to *gmb*of the transistor) compared to its gate-driven counterpart while special fabrication process, such as deep n-well is required to have both nMOS and pMOS transistors operate in the body-driven configuration.

Application of comparator

SAR ADC: The architecture of SAR ADC has depicted in Figure 1, which contains of certain levels of the comparator, DAC having embedded S/H circuit, SAR Control logic circuit, and SAR control logic circuit. The architecture has one comparator block considered being more power-efficient. It

reduces the need for power consumption by not using an Op-Amp circuit. The capacity of Power dissipation receives enhanced using sample rate which is connected using system dissimilar to Flash ADCs wherein dissipation of power could be independent across the rate of sample (Labhane&Prachi , 2015) (Karpe, Prateek , & et al, 2013), and (Pradeep &Mahaveera , 2016).

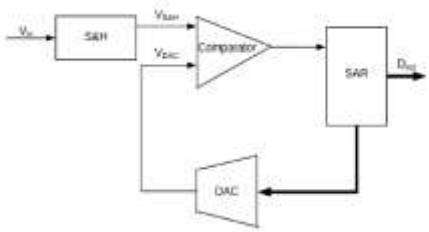


Fig 1Successive Approximation Register Analog to Digital Converter

Advantages: ϖ Medium speed of operation ϖ Mostly digital circuitry ϖ Medium accuracy ϖ Trade-off among the speed and cost ϖ Limited power consumption Limitations: ϖ Accuracy of system relies on accuracy of DAC and comparator ϖ Lower sampling rates ϖ In the instances of higher resolution, it shall be much slower and speed limit of 5Msps The most common DAC architectures in SAR ADC are ϖ R-2R DAC(RDAC) ϖ C-2C DAC(CDAC) CDAC: Good device matching characteristics with higher linearity. Limiting sampling speed and area increases with corresponding resolution increases It has the benefits of reducing the capacitance when compared to the traditional conditions of CDAC, which are binary-weighted. However, they are more sensitive for parasitic capacitances, wherein the non-linearity errors have considered, though they require calibration due to such error conditions. RDAC: Static Power consumption and it required classified S/H circuit, wherein it has only simple architecture and biggest asset in terms of architecture wherein when there is one comparator that consumes lower power for functioning. Also, as it has single OpAmp, the power-hungry requirement significantly reduced. In the other dimension, SAR ADC can rate as the only architecture which deploys a digital circuit to its architecture, which has seen as a crucial part of SAR ADC. SAR logic reflects on the values for reference generation in DAC and leads to digital value integral to the output. The other key block in the process is the SAR logic, wherein the function is profoundly about taking the output of the comparator into account for the generation of binary-weighted references for DAC. A distinct set of DAC architectures enable the similar operation for SAR ADC, in terms of generating appropriate reference voltage for the comparator. Comparative Performance of Various ADCs: The performance of various ADCs is given in Table 1.1 (Bashir, Samiya ,& et al, 2016),(Patel &Hetal , 2012),(Labhane&Prachi , 2015).

Literature

The work (Babayan-Mashhadi& Reza Lotfi, 2013) presented a dynamic comparator for the delay with analytical expressions to discuss the issues in the design of a dynamic comparator. A late design of a dynamic comparator has intended by modifying a doubletailed comparator for small power and great speed of operation with smaller voltages with a simple design for mitigating any delay and some levels of power dissipation. The design is done using 0.18µm CMOS to simulate the circuit. With 1.2V and 0.6V of power supply, the frequency of the new comparator has expanded to 2.5 and 1.1 GHz, with the dissipation of 1.4mW and 153µW of power, respectively. When 1.2 V is applied the probable error of the information alluded counterbalance is 7.8 mV. Kick back noise will be much higher in the range of conditions for the solutions.

Yongsheng Xu et al. [68] have proposed a 4b ADC with novel dynamic comparators. The architecture of this dynamic comparator contributes to low power efficiency, less area and high operating speed. The comparator doesn't use calibration parameters for reducing power consumption. For conventional dynamic comparators, the speed restriction of small LSBs due to the difference between the small charging and discharging times of the first stage and the relatively lengthy charging and discharging periods in the regeneration stage. Here the ADC designed has the highest sampling rate when compared with the conventional architectures.

SedighehHashemi et al. [69] have proposed a pipeline ADC that exhibit interesting mechanisms for metastability which harm the residues and digital output that is created at each stage. The residue may or may not have adequate time to settle, depending on the depth of the metastability. Moreover, a given stage's residues and digital outputs may be inconsistent. The CMOS ADC 8-bit 600MS/s metastabilitybehaviour has been characterized and showed consistent adherence to theoretical results. Philipp Ritter et al. [70], have presented a 6b ADC without track-and-hold, interleaving, or any other digital assistance. Several methods for optimizing energy efficiency are outlined for its implementation in a commonly applicable way. The dynamic comparators have limited dynamic linearity. The Comparator is optimized to have low power consumption. It is observed that the power consumption is a vital attribute in almost all the circuits proposed now a days, here also it is established that low power consumption is attained.

Yonghong Tao et al. [77], have discussed and analysed the comparator offset error in the frequency domain, which is caused due to mismatch of load capacitance present at the output of the latch. Usually static latch comparator is very much sensitive for load capacitance mismatch when compared to the dynamic latched comparator because in the regeneration phase the output nodes of the dynamic comparator are charged to VDD.

A technique called latch interpolation is presented by Jong-In Kim et al. [78], which can minimize the number of latch stages to one fourth of the total in ADC. Clock timing of the second stage latch is adjusted by using intended cascaded latch interpolation. There has also been discussion of issues with the design and robustness of the suggested approach.

A simple solution has been provided for designing a low power dynamic latched comparator by HarijotSingh Bindra et al. [89]. The low power operation of comparator is possible because of the partial discharge of voltage at the pre-amplifier output nodes. The output node has capacitors to eliminate the noise. The analysis showed that noise of pre-amplifier is independent of the transition time and the noise can be minimized by increasing gm/Id for given load capacitance. The total circuit is functioned in the weak inversion region for attaining a low input-referred noise and a low power operation for given load capacitances. By applying tuneable common-mode voltage to the dynamic comparator, the performance of the comparator can be optimized. The dynamic comparator has a large clock delay because it is operated in a weak inversion region. The power consumed for each comparison is independent of the latch transition speed.

Kyoohyun Noh et al. [92] have introduced a dynamic logic switched and a VM switched-off comparator. The suggested solutions for low power circuits declines the switched offset comparator's power loss and the offset or delay synchronization loops, which is a major significant power loss features of new active CMOS rectifiers. The designed comparator uses the biased current again in its place of inserting extra offset current into the standard gate push-pull comparator in order to create uninterruptedly adjustable input-referred offset voltage, thus eliminating the loss of comparator power. The implications of the scaling system on power loss are currently being studied.

Tzu-Yun Wang et al. [93] described a bypass switching based DAC is used in SAR-ADC which also consists of a proximity dynamic comparator. The new dynamic proximity comparator automatically creates the bypass signals. In order to maximize power reduction for sensing different bio potential signals, the bypass window can be altered with a low voltage sensor. The window size of the ADC and dynamic comparator speed are analysed for low power operation in ECG signal recording applications. The SAR logic is simplified for lower power dissipation. The designed ADC is implemented in CMOS 180nm technology with a supply voltage of 0.6V. The ADC achieves ENOB of 9.16 at a sampling rate of 50KS/s by consuming power of 114nw.

Athanasios T. Ramkajet al. [94], have developed a low power dynamic multistage comparator in CMOS 28nm technology. The comparator has three-stage triple latch topology for attaining high gain. The Comparator achieves a sampling rate of 13.5 GB/s with maximum differential amplitude of 5 mVpp, and consumes a power 2.2 mW and has a chip area of 78 μm2.

The new dynamic comparator with a new Transconductance improved latching stage suitable for a high-speed low-power operation has been implemented by YAO WANG et al. [96]. In the cross-coupled inverter latch, the transistors are very well biased to work in strong inversion during the reset

or pre-charge phase of the comparator because the effective trans conductance of the latch is improved at the beginning of comparison phase which pointedly reduces the power consumption and delay. In comparison with the other conventional architectures, the delay and power dissipations are reduced to a reasonable extent.

HaoXu et al. [97] presented a simple analysis of a regenerative comparator, which has played a crucial role in the design of preamplifier, which is present in most of the comparators. A clear, comprehensive analysis has been presented on the advantages and disadvantages of transistor biasing in the circuit. The comparator has operated very well with low noise and low offset when the pre-amplifier is designed well. In comparison to the conventional single tail and double tail comparators, Strong Arm comparator has the merits of speed, noise and low power operation at lower supply voltages.

The work (Malik & Srivastava, 2014)presented a new double tail comparator consisting of CMOS latch and SR latch operated for high frequencies of data transformation, and it has distinguished with the available comparators concerning area, PDP, power dissipation and delay. The power consumption decreases for frequencies higher than 350MHz. The frequency of operation can also be improved from 1.7 GHz to 2.5 GHz with shorter delays applicable for high-speed devices. This shows an improvement in the area at 23.57% compared to the previous best design. The simulations have done in cadence virtuoso spectera with 0.18µm SCL technology. This design is not suitable for low frequencies of less than 200MHZ.

The work (VinodiyaSagar Kumar &Gamad, 2017) In their study has discussed the models of various analysis of CMOS comparators, wherein the scope of low supply voltages are much significant and having higher speed and efficiency, wherein the transient response and DC response have managed as an integral solution. Used Cadence Virtuoso ADE SCL 0.18µm technology tools operated at 1.2V power supply. With 250MHz clock frequency observed, the power utilization of 96.5pw with a propagation delay of 0.56ns. By modifying the applied voltage and aspect ratio the trade-off among speed and power can be solved.

The work (RabieiAhmad , Arman Najafizadeh, & et al, 2015)designed a dynamic regenerative comparator to decrease power dissipation in a pre-amplifier comparator. The speed of the comparator can be improved using a cross-coupled mechanism with little power dissipation and lesser input voltages. With a clock frequency of 3MHz achieved power dissipation about 6nW with 79pS of time delay in 90nm CMOS technology. This circuit finds applications in bio implantable devices and ADCs.

The work (Gao Hao, Peter Baltus, & et al, 2010)proposed a high speed, less power, and low voltage comparator, which takes into account two sets of tail current sense amplifier conditions constituting symmetric SR latch scope. As a result of the increments in the speed and stable output, the design can rely on flash ADC for attaining 5.4-bit resolution, which is effective considering the input signals that are of lower frequency (100 MHz, 124.03mW) and range of power dissipation constituting 1.2 V range of power supply. However, from the experimental studies, it is evident that the model is highly complex and might the condition. The work (Patel Chandrahash& C. S. Veena, 2014)have discussed the scope of using the comparators, which are of open-loop, higher range of comparator speed, regenerative comparator, dynamic comparator and double tail comparators with expressions. From these expressions, the designer can explore the trade-offs during the process of design by considering various parameters. The maximized speed of comparator with power efficiency is essential for managing a low power, higher speed range, and a smaller area of ADC converters.

The work (S.Chandra Pandey, P.Mishra,Rahul Roy, & et al, 2016)proposed a dual-stage Op Amp at ± 1.8V power supply utilizing 0.18µm CMOS technology. The investigation has accomplished for Bandwidth, Phase edge and slew rate, and so on. The Pole isolation miller compensation approach is to improve the gain of the two-stage amplifier. The500nm of slew rate in the case of channel length has considered managing the simulation. The estimations of Cc=8pf and CL=10pf. It has been intended to show a solidarity attain frequency of 18.2MHz and secured a gain of 71.27dB. The slew rate will reduce if the channel length is modified. The work (Kavyashree C. L., M. Hemambika, & et al, 2017)designed a CMOS amplifier with two stages in 90nm CMOS with ±1V of power supply. Analyzed the various specifications such as slew rate, power dissipation, and phase margin, a gain of op-amp but concentrating on the gain of the amplifier. Implemented the design in cadence virtuoso

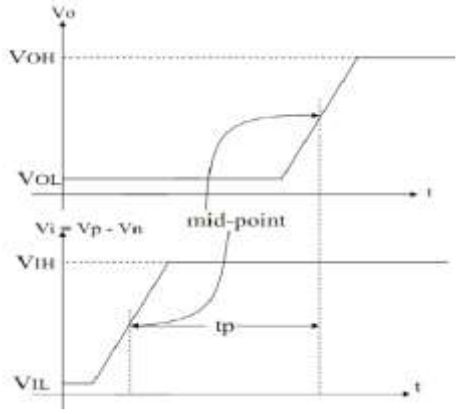
and obtained the gain as 84dB, 56° phase margin with 38.02µW of power dissipation. The work (Kasundra, Ravia, & et al, 2016)presented a single-stage and two-stage op-amp designs using 0.18µm using NGSpice and observed the output as 72dB gain,133v/µs slew rate, phase margin of 51° with 77dB CMRR at 3.3 V power supply for a two-stage op-amp. Phase margin decreased in two-stage op-amp due to scaling. The work (Bandyopadhyay, Deep Mukherjee, & et al, 2014)presented a two-phase opamp through minimum scaling of device parameters due to which the current, power, and area can reduce. To improve the Stability Miller compensation procedure has used. Observed a gain of 36.74dB with power consumption of 0.804mw, UGB=16.5MHz,
CMRR=133.69dB and PSRR=179.3dB at 2.5V supply. The compensation capacitance is Cc=3pf with a load capacitance of CL=10pf. To decrease the size of the circuit capacitance values can be minimized. Phase margin has degraded, and the large value of compensation capacitor has used. The work (VermaAnchal, Deepak Sharma, & et al, 2013)in their research studies have discussed the scope of the two-stage op-amp, which constitutes conditions of differential gain, biasing network conditions, and the gain stage conditions. The gain of 96dB, 700° phase margin with UGB of 4.416MHz have obtained with ±2.5V power supply utilizing LT spice tools. It is imperative from the conclusion that the phase margin is relatively high leading to ringing in the output.

Dynamic characteristics of the Comparator

The comparator's dynamic characteristics consist of small as well as large signal behaviour. At this point we do not know how long it will take for a comparator to respond to the input differential data.

a. Propagation delay

The propagation delay can be defined as the speed at which the Comparator responds to the applied input data. Simply it is the interval between input and output. The propagation delay of the comparator is shown in Figure 4.4.



Propagation delay of the Comparator

b. Slew rate The slew rate of the Comparator is based on the output waveform slope during the fall or rise time of the load capacitance. But it is limited by the current source or sink capability for charging the output of the load capacitor. **c. Speed** The inverse of the Propagation delay value is termed as Speed.

$$\text{Speed} = \frac{1}{\text{Propagation delay}}$$

LOW POWER TECHNIQUE:

Advancement feature size and limit voltage have been scaling for a significant long time for achieving high thickness and unrivaled. In light of this development design, transistor spillage compel has extended exponentially [4]. As the part measure gets the opportunity to be smaller, shorter occupy lengths bring extended sub-edge spillage current through a transistor amid it is off. We can achieve extended sub-limit spillage current in light of the fact that transistors can't be murdered completely at the low edge voltage. Subsequently, static power usage, i.e., spill control dispersal, has transform into a basic piece of total power use for silicon advancements. There are VLSI techniques to less spillage control. Each methodology give a successful way to deal with decrease spillage control; however

obstacles of each framework compel usage of each technique. We proposed other technique, to low-spillage control VLSI makers.

Dual Sleep:

Double rest system uses the advantage of using the two extra draw up and two extra draw down transistors in rest mode either in OFF state or in ON state. As shown in the Fig. 4.5.3 the twofold rest bit can be made fundamental to all reason equipment, less number of transistors is required to apply a specific method of reasoning circuit.

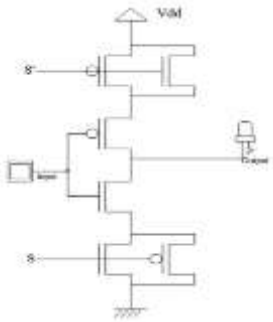


Fig : Dual Sleep

Proposed sleep controlled Double-Tail comparator:

The main idea of the proposed comparator is to reduce the power consumption. For this purpose we have applied a sleep transistor technique and two control transistors (*M*c1 and *M*c2) have been added to the first stage in parallel to *M3/M*4 transistors but in a cross-coupled manner to improve the speed of comparator. As shown in the above Fig. the task of the proposed rest controlled double tail comparator, amid reset stage. When CLK = in3 = 0, Ntail1 and Ntail2 are off, P1 and P2 transistors pulls both f1 and f2 hubs to VDD, consequently transistors Pc1 and Pc2 are cut off. Middle stage arrange transistors, NR1 and NR2, reset both lock yields to ground. Amid basic leadership stage (CLK = in3 = VDD, Ntail1, andNtail2 are ON). The rest transistor doesn't permit VDD to lock circuit. The measure of spillage control lessens unimportantly little contrasted with controlled double tail comparator.

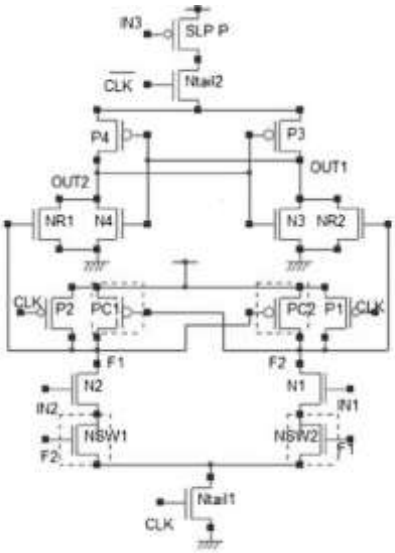


Fig schematic of Proposed sleep controlled dual tail comparator

RESULTS

The dynamic double tail comparator without sleep transistor circuit was simulated using Cadence Virtuoso tool with 45nm CMOS technology. The supply voltage used in simulation is 1V. The waveforms of the this comparator are shown below:

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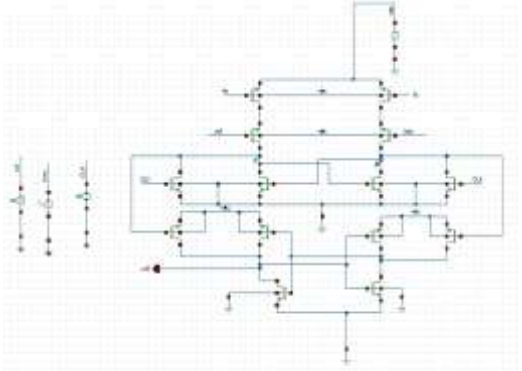

Fig : Dynamic double tail comparator without sleep transistor technique

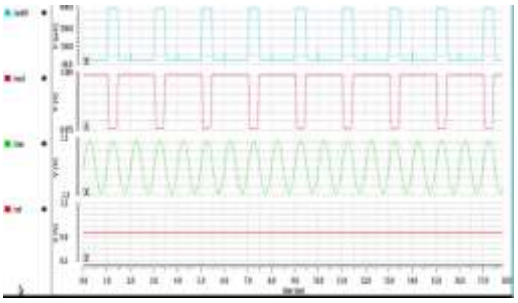

Fig : waveforms of comparator without sleep transistor technique

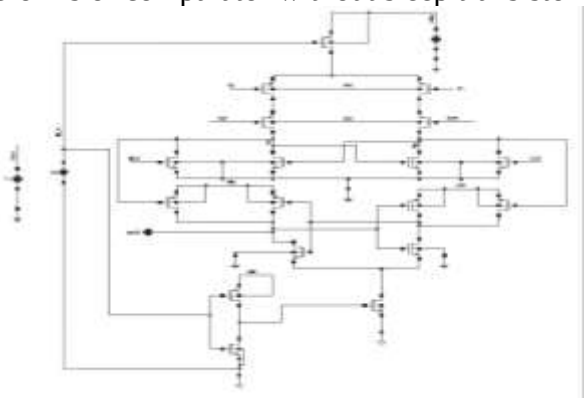

Fig : proposed dynamic double tail comparator with sleep transistor technique

The proposed dynamic double tail comparator with sleep transistor technique was simulated using Cadence Virtuoso tool with 45nm CMOS technology. The supply voltage used in simulation is 1V. The waveforms of the proposed dynamic double tail comparator with sleep transistor technique are shown below:

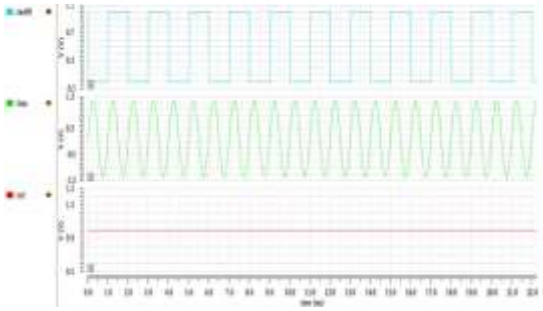

Fig : Waveforms of dynamic comparator with sleep transistor technique

Comparison Table:

Comparator type	Power Consumption
Comparatorwithout sleep transistor technique	**40.56uW**
Comparator with sleep transistor technique	**36.56nW**

CONCLUSION

Double tail comparator with sleep transistor technique is designed and simulated using 45nm CMOS Technology. From the simulated results it is observed that the power of the dynamic double tail comparator with sleep transistor technique is reduced which is comparatively less than the comparator without sleep transistor technique. The average power consumption of the proposed dynamic double tail comparator with sleep transistor technique is calculated as 36.56nW. The average power consumption of the dynamic double tail comparator without sleep transistor technique is calculated as 40.56uW. Hence the power consumption is reduced as compared with the dynamic comparator without sleep transistor technique.

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