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ARITHMETIC LOGIC UNITS USING REVERSIBLE CIRCUITS: A REVIEW

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ABSTRACT:-
The increasing demand for high-speed, portable electronic devices has led to the design of processors with reduced size, time, and power consumption. The arithmetic logic unit is the fundamental block of the processor. The performance of the ALU has direct impact on the performance of the processor. To increase the speed of the processor, the speed of the arithmetic logic unit has to be increased. An arithmetic and logic unit design which can perform arithmetic functions such as addition, subtraction, multiplication, division and logic functions such as AND, OR, NOT, NAND, NOR, EXOR, EXNOR, BUFFER with inputs and outputs format is designed. In this paper the study of different research paper based on arithmetic logic unit and reversible logic gate. It is also explain the objective and scope of the future work.

Keywords:-
Arithmetic Logic Units, Addition, Sub-tractor, Logic Function

I. INTRODUCTION

The necessity for high-speed processors and the need for processors to deal with intricate processes have led to the incorporation of many processor cores into a single chip. The technique of producing an integrated circuit by combining multiple transistors into a single chip is known as very-large-scale integration (VLSI). The integrated circuits had restrictions in functionality before the introduction of very-large-scale integration. With the introduction of VLSI technology single IC can be designed to perform all the functions. The performance of the IC is characterized by delay, power dissipation, and area [1]. The major contribution to the delay is the propagation delay caused by the interconnections in the critical path of a circuit. In addition to it, the temperature, voltage, and process parameters also affects delay. The shorter propagation delay will result in a high-speed circuit [2]. The power dissipation per gate should be maintained as low as possible to meet the power requirements within limits. Power dissipation is characterized as static power dissipation, dynamic power dissipation, and short circuit power dissipation depending on the source. Static power dissipation is produced by leakage in stable states, dynamic power dissipation is the energy consumed during switching operations, and short circuit power dissipation is an element of dynamic power dissipation due to the direct current flowing among supply rails. The circuit area should be studied to estimate and optimize the cost of silicon needed to implement the circuit, packaging cost, average interconnect length [3, 4]. Area can be reduced by advanced circuit design techniques and processing technology to achieve minimum device size and through careful chip layout. A processor has an arithmetic and logic unit (ALU), cache, registers, buses, clock and control unit. The control unit fetches, decodes and implements instructions and provides signals to regulate the data movement. The registers are high speed memory units confined within processor to stock small information such as address of instruction and results of calculation [5]. The cache is a modest high-speed memory chip embedded into the CPU that stores data and instructions that the processor is anticipated to subsequent processing. A bus is a high-speed internal link that connects the CPU to other components to transfer control signals and data. By sending a regular electric pulse, a clock is employed to synchronize the components. The ALU is the processor's primary unit. It conducts arithmetic functions such as addition, subtraction, multiplication, division and logic functions such as AND, OR, NOT, NAND, NOR, EXOR, EXNOR, and Buffer. The performance of the ALU has direct impact on the processor's performance [6]. The

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arithmetic logic unit's speed must be improved to improve the processor's speed. The need for high speed, portable electronic devices has led to the design of processors with reduced size, time and power consumption. So, by optimizing the ALU, the processor can be optimized where our proposed ALU will be useful.

II. LITERATURE REVIEW

In [7], have work targets streamlining the equipment execution of the SubBytes and converse SubBytes activities in the high level encryption standard (AES). All building blocks in the S-box (and inverse S-box) of the SubBytes (and inverse SubBytes) transformation are optimized using composite field arithmetic (CFA) in response to this. A joint plan of S-box and backwards S-box is likewise proposed to additional improve the region effectiveness. In particular, there is a decrease in the area of the multiplier in the Galois composite field GF ((22)2). The squaring and duplication with consistent λ in GF ((22)2) are consolidated and improved also. In addition, multiplicative inversion is manually optimized. Moreover, the S-box and reverse S-box are joined and improved utilizing the preprocessing and post processing modules. To build the throughput, a decent and pipelined engineering is determined. Utilizing the proposed design, a throughput of 5.79 Gbps for the S-box can be accomplished on Virtex-6 XC6VLX240T and 10% better than the customary work. As per the ASIC execution result, the proposed plan can in any case accomplish the most elevated region effectiveness and roughly 30% better than ordinary works utilizing TSMC 90nm cycle.

In [8], due to extensive device scaling, semiconductor devices have seen significant improvements in performance and speed, while power dissipation has emerged as a major concern. As the scaling of gadget has been arrived at its limits the advancement could be the arising innovation i.e., Reversible registering in VLSI industry. Reversible logic circuits benefit greatly from this technology's lack of power dissipation. The ALU is significant part in the framework and it is utilized in the applications like PCs, mobiles, and number crunchers. The 32 Digit number juggling rationale unit is planned utilizing Verilog Equipment Depiction Language with activities, for example, AND rationale, OR rationale, Full Adder utilizing the slightest bit ALU. The reversible ALU can work quickly as contrasted and irreversible ALU. The area, delay, and power dissipation of reversible logic gates are reduced. The AND and OR gates for each one-bit ALU are replaced by an ALU made of reversible logic gates designed in this paper using the Toffoli, Fredkin, and Peres Gate. Modelsim Altera 6.3g is used for all logic, and Xilinx ISE 14.7 is used for the synthesis. The planned ALU utilizing reversible rationale diminishes the region around 34% and delay around 48.91%.

In [9], QCA innovation is viewed as one of the most appropriate substitutions to decrease the CMOS-based advanced circuit plan issues at the nanoscale because of its little size, quick, inactivity and exceptionally low power utilization. The arithmetic logic unit (ALU), also known as the microprocessor's heart, is one of the most important components. This paper presents a QCA innovation based reversible ALU unit utilizing fundamental reversible blocks and a clever reversible block in particular BS1 Block. The proposed block performs rationale and math activities in the proposed conspire. The recreations of the proposed plan are done by QCA Creator. As per the reproduced results, the proposed structure has a 35%, 27% and 30% improvement in quantum cost, the quantity of cells and the involved region in contrast with the past directed explores, separately.

In [10], the execution of AES S-boxes is one of the most broadly concentrated on areas of cryptography. In this paper, we propose three new equipment plans for the AES S-confine that can serve the forward, opposite and joined information ways. Every one of these plans addresses the littlest AES S-confine at any point proposed its individual classification. We accomplish this objective by utilizing new pinnacle field portrayal over typical bases and upgrading every single block inside the three proposed structures. Our intricacy examination and ASIC amalgamation brings about the CMOS STM 65 nm, as well as the NanGate 15 nm advancements, show that our plans outflank their partners concerning region and power.

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In [11], an effective cryptographic algorithm known as Advanced Encryption Standard (AES) can be used to ensure the safety of electronic data. It must continue to resist the majority of attacks. In this work, AES-128 encryption iterative engineering is intended to accomplish least region and less equipment use. By incorporating a reworked S-box structure into the AES algorithm, reduced area is achieved. Moreover, equipment usage is limited by consolidating the Vedic multiplier in the Blend segment change of the AES Encryption process. The proposed encryption design is of 128-digit size and was executed on the Xilinx Austere FPGA series, to be specific, Straightforward 3, Virtex-4 and Virtex-5 gadgets. The improvement result displays that the proposed S-box method has a more modest region than other existing traditional works.

In [12], this short presents an effective brought together equipment for exceptional validated encryptions with related information (AEADs). Albeit some major AEADs share a few key parts (e.g., high level encryption standard (AES), block binding, and XOR-Encryption-XOR (XEX) plot), each AEAD is outfitted with a remarkable method of activity as well as sub-capabilities, which makes it challenging to coordinate different AEADs in an equipment productively. The proposed equipment in this brief proficiently brings together the key parts to play out a bunch of AEADs with negligible region and power overheads. The given AEAD algorithm directs the adaptation of the proposed configurable data path to a set of peripheral operations, such as block chaining and XEX. In this short, we likewise exhibit the legitimacy of the proposed equipment through a trial configuration adjusted to four AES-based AEADs. As a result, we confirm that the proposed hardware can perform the four AEADs with comparable throughput and power consumption to the dedicated AEAD hardware while taking up significantly less space. In addition, we verified that the throughput and power consumption of the proposed hardware are superior to those of software implemented on a general-purpose processor.

In [13], reversible logic circuits can be used in place of conventional logic circuits to solve the problem of energy loss in digital circuit design. The most promising technology is reversibility. The digital system is implemented using conventional gates like AND&OR gates, which dissipate a significant amount of energy in the form of bits that become erased during logical operation. In today's world, ALU is one of the most critical components of any system that is used in numerous devices such as computers, smartphones, calculators, and so on. In this paper the plan of the slightest bit reversible ALU utilizing reversible rationale entryway is proposed. The proposed ALU is dissected on FPGA SPARTAN6 gadget. The propagation delay, quantum cost, and garbage outputs of the proposed design are compared to one another. In this paper the 4-cycle reversible ALU is additionally configuration on proposed 1-digit reversible ALU engineering.

In [14], a method for building the Arithmetic Logic Unit (ALU) using reversible logic gates as logic components is proposed in this paper. A reversible ALU with the same function as a traditional ALU is constructed by employing reversible logic gates rather than traditional logic gates like AND gates and OR gates. The introduced reversible ALU diminishes the data pieces' utilization and misfortune by reusing the rationale data bits legitimately and understands the objective of bringing down influence utilization.

In [15], ALU is utilized in number juggling, coherent capability in all processor. Additionally, it is a crucial subsystem in the design of digital systems. One of any system's most crucial components, the ALU is found in numerous devices like calculators, smartphones, and computers. A 32-digit ALU was planned utilizing Verilog HDL with the consistent doors, for example, AND as well as for every the slightest bit ALU circuit. In Xilinx, the design was put into action. It can work quick than the ALU processor utilizing less power. A high-performance processor's ALU and cache memory design were investigated. Power consumption is higher in ALU designed with non-reversible logic gates. So there is a requirement for lesser power utilization and the reversible rationale has been assuming essential part during late years for low power VLSI Plan procedures. Power dissipation and consumption can be reduced with this method. This paper contrasts ALU architecture with normal logic gates with an implementation of ALU based on reversible logic. Every one of the modules are recreated in modelsim

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SE 6.4c and combined utilizing Xilinx ISE 14.5. The implementation of an ALU based on reversible logic reduces power consumption during operations by approximately 5.1 percentage points, while an ALU designed with non-reversible logic gates consumes approximately 0.312 mW more power.

In [16], the reversible logic design plays a great role in different design technologies like CMOS, bioinformatics, optical information processing, nano devices, cryptography etc. All the outputs of the reversible gate perform some specific set of Boolean functions. So many research works have already been done on this reversible technique. New gate, namely SS reversible logic gate, its input-output table and execution of half adder subtractor and full adder-subtractor was presented [17]. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. In Conventional digital circuits, the main cause of power dissipation is the disposal of bits of information while the logical operations are being carried out, So if these circuits are designed with reversible logic, the bit loss can be preserved. As 1-bit Full Adder is the elementary unit in almost all the digital circuits, So this paper gives the Comparative Analysis of 1 bit Full Adder circuit using reversible logic in order to find out the most efficient circuit in comparison to existing ones as in terms of Dynamic Power, Leakage Power, Area and Delay [18].

In [19], all the circuits were designed with Verilog HDL and has been simulated Using NC-SIM. The RTL analysis was carried out with RTL compiler 14.01 by Cadence for Power, Area and Delay at 90nm and 45nm technology for both fast and slow library. Reversible methodology essentially expects to overhaul any advanced circuit with reversible structure units. Here, we propose a productive way to deal with structure N-bit Adder/subtractor utilizing reversible approach. In light of proposed N-bit adder/Subtractor plan we have likewise thought about 4-bit, 8-bit and 16-bit circuits with the current structures. Proposed plans are reproduced and incorporated with Xilinx Spartan 3E for Device XC3S500E at 200 MHz recurrence the Circuit has been executed and mimicked utilizing Xilinx programming. In this way, other than including and subtracting numbers, ALUs regularly handle the duplication of two whole numbers; following the outcome is additionally a number. ALUs normally don't perform division operations, since the outcome might be a part, or a "coasting point" number. While the ALU is a central part of all processors, the outline and capacity of an ALU may shift between various processor models.

In [20], the ALU is significant part in the framework and it is utilized in the applications like PCs, mobiles, and mini-computers. The 32 Bit number-crunching rationale unit is planned utilizing Verilog Hardware Description Language with tasks, for example, AND rationale, OR rationale, Full Adder utilizing One piece ALU. The reversible ALU can work quickly as contrasted and irreversible ALU. Reversible rationale entryways diminish power dispersal, postponement and region. Presents an ALU planned of reversible rationale doors utilizing Toffoli, Fredkin, and Peres Gate which replaces the and additionally entryway for every the slightest bit ALU. Every one of the rationales is performed utilizing the virtual products Modelsim Altera 6.3g and the blend utilizing Xilinx ISE 14.7. The planned ALU utilizing reversible rationale decreases the region around 34% and delay around 48.91%.

In [21], one of the principle parts of chip is the ALU and as such, it goes about as the core of microchips. This paper presents a QCA innovation based reversible ALU unit utilizing essential reversible squares and an original reversible square in particular BS1 Block. The proposed block performs rationale and number-crunching tasks in the proposed plot. The recreations of the proposed plan are done by QCA Designer. As per the mimicked outcomes, the proposed structure has a 35%, 27% and 30% improvement in quantum cost, the quantity of cells and the involved region in contrast with the past led explores, separately. It could be utilized for planning ultra-low power circuits, which will assist with lessening the complete energy utilization around the world. Testing of these circuits has additionally been a main pressing issue to approve their usefulness.

In [22], this Paper presents an original plan of Arithmetic Logic Unit (ALU) that can be adaptable up to N number of pieces. The plan interaction uses the properties of Toffoli and Fredkin doors to make the circuit equality protecting which shows its in-assembled testability highlight. Proposed design gives full inclusion of single piece flaws in the circuit. The plan and execution is performed over

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reversible circuit analyzer for getting working expenses as far as number of information sources, door count, quantum cost, trash yields and ancilla inputs. It has wide applications in cutting edge registering, low power CMOS plan, Optical data handling, DNA registering, bio data, quantum calculation and nanotechnology.

In [23], computerized framework executed by utilizing customary doors like AND as well as entryways disperse a significant sum of energy as pieces which gets eradicated during coherent tasks. This issue of energy misfortune can be address by utilizing reversible rationale circuits instead of customary circuits. The most promising advancement in digital circuit design is reversibility. In today's world, the ALU is one of the most crucial components of any system that is used in numerous devices like computers, smartphones, calculators, and so on. Reversible logic gates are used to propose the design of a 1-bit reversible ALU in this paper. The proposed ALU is examined on FPGA SPARTAN6 gadget. The proposed plan is looked at as far as engendering delay, quantum cost and trash yields. In this paper the 4-cycle reversible ALU is likewise configuration on proposed 1-digit reversible ALU design.

In [24], quantum Registering has arisen as a cutting edge type of processing involving reversible rationale as its premise. Aside from quantum registering, Reversible rationale and its rationale blend has been getting extensive adulation in applications, for example, low power CMOS plan, nanotechnology, DNA processing and optical figuring too. This paper propounds a streamlined reversible full viper subtractor configuration called "WG door". By reducing its parameters, such as quantum cost, garbage outputs, and so on, the design of reversible gates can be improved. yet, this proposed entryway is enhanced as far as quantum cost and can be utilized in different snake subtractor circuits. The reversible logic can be used to construct even more complex circuits, despite the fact that this paper only provides a basic component for performing arithmetic addition and subtraction.

In [25], reversible rationale is a lot of popular for the future processing advances as they are known to deliver low power scattering having its applications in Low Power CMOS, Quantum Figuring, Nanotechnology, and Optical Registering. In many computational units, adders and multipliers are fundamental building blocks. Using a modified Baugh-Wooley approach and standard reversible logic gates/cells based on complementary pass-transistor logic, we have presented and implemented a reversible Wallace signed multiplier circuit in an ASIC in this paper. Simulations, a layout vs. schematic check, and a design rule check were used to validate our findings. In terms of hardware complexity, garbage outputs, number of gates, constant inputs, and transistors required, it is demonstrated that the proposed multiplier performs better and is more optimized than its predecessors. It has additionally been displayed in Rhythm's devices that the reversible multiplier beat the irreversible multiplier with regards to control dispersal.

In [26], Moore's Law says that transistors are getting smaller and more common as nanotechnology advances. As the transistor heat dissipation reaches the Land Auer limit, researchers are becoming increasingly concerned about the issue of heat dissipation. Reversible rationale is anticipated to be an option in contrast to ordinary registering because of lesser energy scattering and dramatically quicker critical thinking limit. Taking into account a four-level quantum system, the well-known NCV library and the recently released NCV-|v1> library are combined in this paper to create a reversible ripple-carry adder. The proposed adder's results are compared to those of previous ripple-carry adder designs. It then, at that point, investigates the plan of an expense enhanced reversible ALU by changing the above snake. At long last, an examination of the proposed ALU is made with one of the most recent reversible ALU plans.

In [27], reversible rationale is one of the main issues at present time and it has various regions for its application. The main goals of designing reversible logic are to reduce the number of garbage outputs, circuit depth, and quantum cost. Another reversible entryway Machine gear-piece is proposed in this paper. This paper also shows how the reversible COG gate makes it simple to implement a 4-bit arithmetic circuit for 8 operations.

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In [28], reversible computing has emerged as one of the most effective and well-known methods in recent years for the design of low-power circuits. In this paper, reversible Number-crunching and Rationale Unit (ALU) is intended to show its significant ramifications on the Focal Handling Unit (CPU).In this paper, two kinds of reversible ALU plans are proposed and confirmed utilizing Altera Quartus II programming. In the proposed plans, eight number-crunching and four consistent tasks are performed. In the proposed plan 1, Peres Full Snake Entryway (PFAG) is utilized in reversible ALU plan and HNG door is utilized as a viper rationale circuit in the proposed ALU plan 2. Quantum cost, propagation delay, the number of gates, and garbage output are all examined and compared for the two proposed designs. The recreation results show that the proposed reversible ALU plan 2 beats the proposed reversible ALU plan 1 and traditional ALU plan.

In [29], reversible rationale is broadly being considered as the potential rationale configuration style for execution in current nanotechnology and quantum registering with negligible effect on actual entropy. Ongoing advances in reversible rationale consider further developed quantum PC calculations and plans for relating PC models. The design of reversible logic gate structures and arithmetic units has received significant attention in the literature; however, the design of reversible ALUs has received relatively little attention. In this paper, we propose the plan of two programmable reversible rationale door structures designated at ALU execution and their utilization in the acknowledgment of a proficient reversible ALU is illustrated. The proposed ALU configuration is checked and its benefits over the just existing ALU configuration are quantitatively examined.

In [30], a design principle for microprocessors known as the Reduced Instruction Set Computer (RISC) favors a smaller, simpler set of instructions that all execute in the same amount of time. RISC engineering is utilized across an extensive variety of stages from PDAs to super-PCs. In this paper the social plan and utilitarian qualities of 16-digit RISC processor is proposed, which uses least practical units without settling in execution. The Harvard architecture, which has separate data memory and instruction memory, serves as the basis for the design. The guidance word length is 24-bit wide. The processor upholds 16 guidelines with three tending to modes. It has 16 universally useful registers.

In [31], each register can store 16-digit information. The processor has 16-cycle ALU fit for performing 11 arithmetical and intelligent tasks. The processor likewise consolidates a banner register which demonstrates convey, zero and equality status of the outcome. Every one of the modules in the configuration are coded in Verilog. The singular modules are planned and tried at each degree of execution lastly coordinated in a high level module by fitting planning. The plan passage and union is finished utilizing Xilinx ISE 10.1 instrument what's more, reproduction results are confirmed utilizing Modelsim 10.2.

In [32], presently days the majority of the circuits which will be intended to play out a particular or security basic tasks are chiefly founded on the computerized space, where microchips and microcontrollers assumes a significant part to plan these advanced circuits. ALU is the core of these processors. By enhancing this co-processor an exceptionally effective advanced processor can be gotten. So this paper is completely dedicated to configuration speed, energy and power productive Math Rationale Unit. The speed of the multiplication unit has a significant impact on the speed of the ALU. There are so many duplication strategies have been contrived at algorithmic and primary level. After an exhaustive report and profound examination we have found that Vedic Urdhva Triyambakam duplication calculation is the best calculation as it creates halfway items in the equal way. In this paper we have proposed another tree duplication structure based engineering to plan this Vedic multiplier.

In [33], the divide and conquer strategy was used to produce products that were only partially generated. For the expansion of to some degree created items another expansion tree structure has been proposed. It gives better speed in correlation Exhibit, Corner, Wallace, Changed Stall Wallace, Karatsuba and Vedic Karatsuba Multiplier as well as it is quicker than Vedic multiplier. Subsequent to coordinating these modules we have gotten the speed, energy and power productive ALU. Xilinx ISE 9.2i software was used to synthesize and simulate the proposed Arithmetic Logic Unit, which is coded in Verilog HDL.

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III.REVERSIBLE GATE

In the existing literature, there are many reversible gates such as the Feynman gate and also the Fredkin gate. The amount of 1x1 and 2x2 reversible gates required to design a 3x3 reversible gate from 1x1 and 2x2 reversible gates is termed the quantum cost of that gate. The quantum cost of all 1x1 and 2x2 reversible gates are considered as unity [34, 35]. The 3x3 reversible gates are typically implemented using 1x1 NOT gate and 2x2 reversible gates like Controlled-V and Controlled-V^+(V is square-root of NOT gate and V^+ is its hermitian) and Feynman gate also referred to as Controlled NOT gate (CNOT).

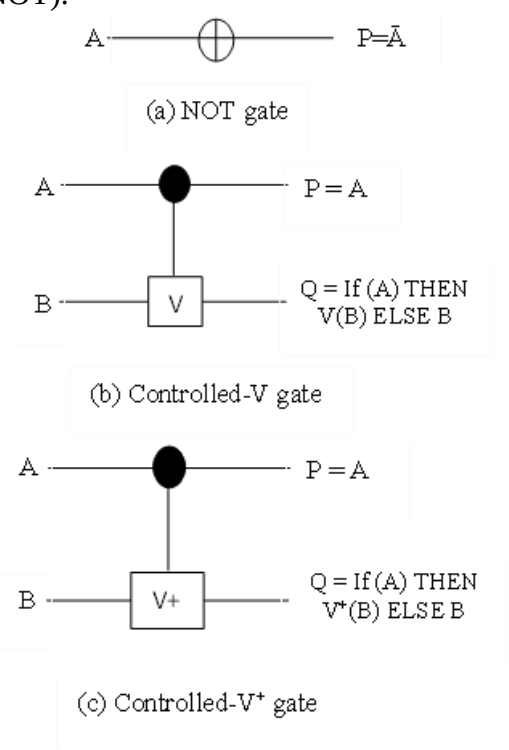
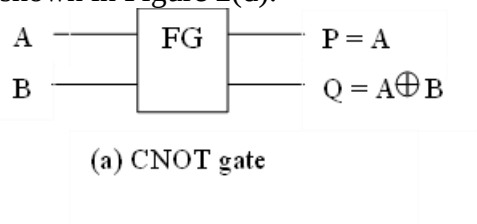


Figure 1: NOT, Controlled-V and Controlled-V+ Gates

The NOT gate is 1x1 and 2x2 gate represented as shown in figure 1. Since it's a 1x1 gate, its quantum cost is unity [36].

Feynman Gate (CNOT Gate)

The Feynman gate (FG) or the controlled-NOT gate (CNOT) may be a 2-inputs and 2-outputs reversible gate with the mapping (A, B) to (P=A, Q=A⊕B). Here A is that the dominant input and B is that the controlled input; P, alphabetic character is that the 2 outputs. Since the Feynman gate may be a 2x2 reversible gate, it's a quantum value of one [37]. Figure 2(a) and 2(b) shows the diagram and therefore the quantum illustration of the Feynman gate. Fan-out isn't allowed in reversible logic. Feynman gate is useful during this look upon it are often used for repetition the signal therefore avoiding the fan-out drawback as shown in Figure 2(c). It may also be used for generating the complement of a given input as shown in Figure 2(d).



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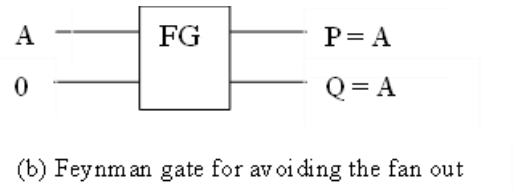

(b) Feynman gate for avoiding the fan out

Figure 2: CNOT gate, its Quantum Implementation and its useful Properties

Fredkin Gate

Fredkin gate is a 3x3 reversible logic gate with 3 inputs and 3 outputs. Figure 3 (a) shows the diagram of a Fredkin gate. The Fredkin gate maps (A, B, C) to (P=A, Q = A'B + AC, R = AB + A'C), where A, B, C are the inputs and P, Q, Rare the outputs, respectively. A Fredkin gate will work as 2:1 MUX, because it is ready to swap its different 2 inputs depending on the value of its first input [38, 39].

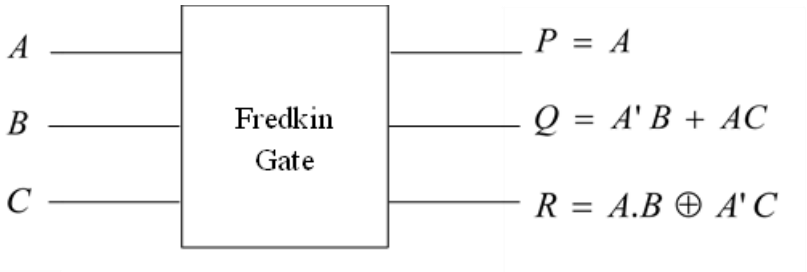

Figure 3 (a): Block Diagram Fredkin Gate

IV. OBJECTIVE AND SCOPE

Objective

- To gain a thorough understanding of reversible Combinational and Sequential circuits and their working principles.
- To design a reversible Combinational Arithmetic Logic Unit using multiplexers, de- multiplexers, encoders, decoders, adders, and subtractors with the aid of different reversible gates, optimizing design parameters such as QC, GO, CI, and GC.
- To design a reversible Sequential Arithmetic Logic Unit using delay flip-flops, registers, comparators, counters, and different reversible gates, optimizing design parameters such as QC, GO, CI, and GC.
- To integrate the design of both Combinational and Sequential Arithmetic Logic Units into a hybrid design using different programmable reversible gates.
- To analyze and evaluate the performance of the designed circuits based on metrics such as speed, power consumption, and area utilization.

Scope

The scope of this proposed thesis is to investigate the design, synthesis, and testing of reversible logic circuits for ultra-low power applications. The primary motivation for adopting reversible logic lies in its potential to provide a methodology for designing circuits that consume less power than the KTln2 limit for emerging nanotechnologies. However, since most commonly used gates in digital design are not reversible, a set of reversible gates is needed to design such circuits [40, 41].

The research will focus on developing new design and synthesis methods for the realization of reversible circuits, including optimization of parameters such as the number of reversible gates, ancilla inputs, garbage outputs, quantum cost, and delay. A synthesis framework will also be developed to optimize multiple parameters simultaneously. The proposed research aims to contribute to the wider adoption of reversible computing and enable the development of energy-efficient and sustainable computing systems for emerging technologies [42].

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V. RESEARCH INVESTIGATION

The design methodology is as described in the figure. The design flow is divided into the following steps:

i. The designer specifies the design requirement such as the parameters to optimize (number of gates, number of ancilla inputs, garbage outputs, quantum cost, delay, etc.) along with the design scheme.

ii. Create a library of all the reversible gates coded in HDL such as the Fredkin gate, the Toffoli gate, the Peres gate, the Feynman gate etc. If a new reversible gate is proposed in the literature, it can be easily added to the library [43].

iii. The HDL code of the desired design is generated. The test benches needs to verify the functional correctness of the design are also generated.

iv. The functional verification of HDL codes is done using standard HDL simulators such as ModelSim/ ISim simulators. The waveforms are to be generated [44].

v. Synthesis of the HDL code is generated by the Xilinx XST synthesizer. The RTL schematic of the design is generated by the synthesizer with various reports such as delay, number of slices occupied and power dissipation.

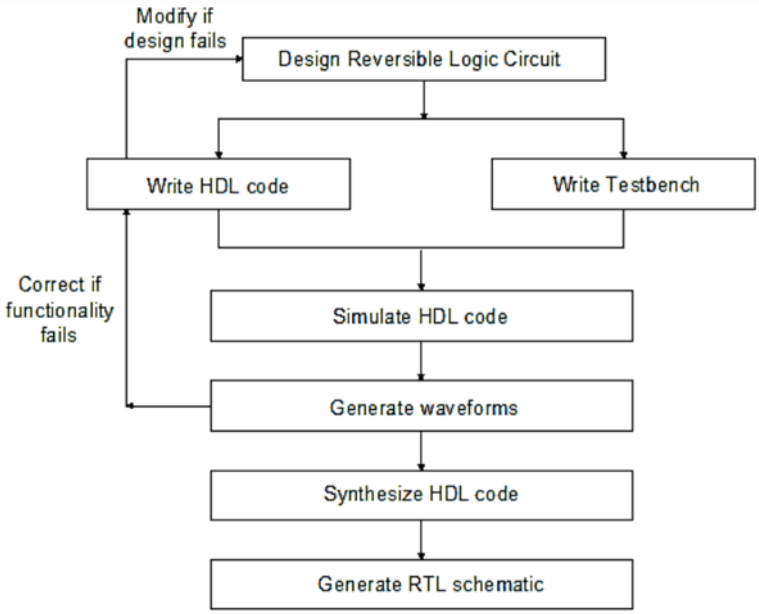

Figure 4: Design flow of reversible logic circuits

VI. SIMULATION RESULTS

The decoder is a collection of logic gates which are arranged in a specific way so that, for an input combination, all outputs are low except one. Many devices for processing used combinational circuit. Control unit is very important block in reversible decoder and control unit work as an efficient instruction decoder, which is used ability to decode the information and it's also control many task, ability to execute the instruction per cycle [45].

2×4 RD

HL gate through constructed 2×4 RD is discussed in Fig. 5. HL Gate in 4x4 reversible logic requires two logical inputs A, B and two constant inputs consisting of only one gate without any garbage output. HL gate having quantum cost as 7. HL gate implementation is consisting of two inputs and generate four outputs are AB, AB', A'B and A'B' is shown in Fig. 5.

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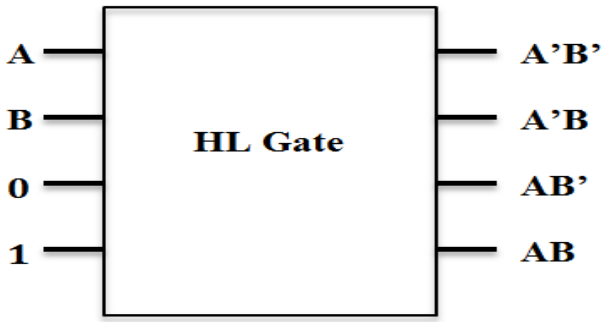

Figure 5: Implemented 2×4 RD

3×8 RD

Here 3×8 RD has been implemented but at first, proposes a 2×4 RD. Implemented 3×8 RD is built by using 2×4 RD, which was implemented by using HL gate and four R gates is shown in Fig. 6. There 3×8 RD consisting of two inputs (A, B, C) and eight outputs i.e., Yi (i = 0, 1... 7). The output equation for 3×8RD is given by following expressions: Y0 = A'B'C', Y1 = A'B'C, Y_2 = A'BC', Y_3 = A'BC, Y_4 = AB'C', Y_5 = AB'C, Y_6 = ABC', Y_7 = ABC. Our main target is achieve the better result and improvements in terms of design parameters such as gate count, quantum cost, garbage output, constant input and total cost as compared to same criteria with existing approaches [46, 47].

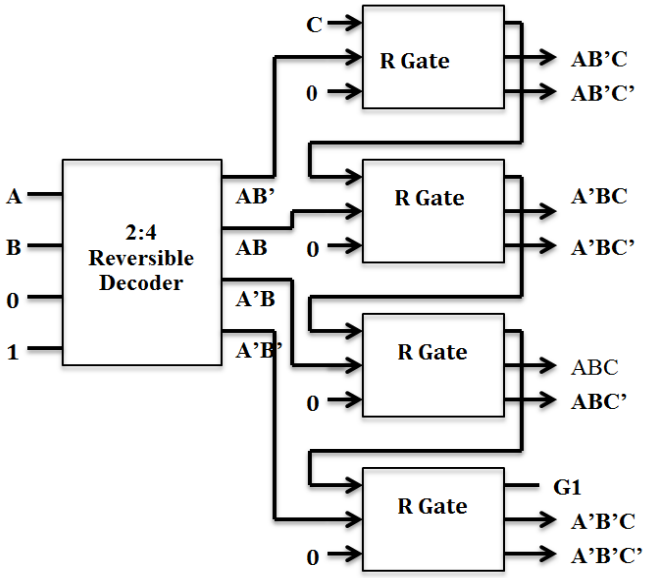

Figure 6: Implemented 3×8 RD

There is a further scope of extending the design to 4:16 and so on up to n-to-2^n reversible decoder, which takes n bit inputs combination and gives out the output addresses by that input combination for each output, corresponds to only one input respectively. This figure 7 shows the VTS of 2×4.RD. Here 'D0', 'D1' is input of 2×4 RD and the output is of maximum four Z1, Z2, Z3 and Z4.

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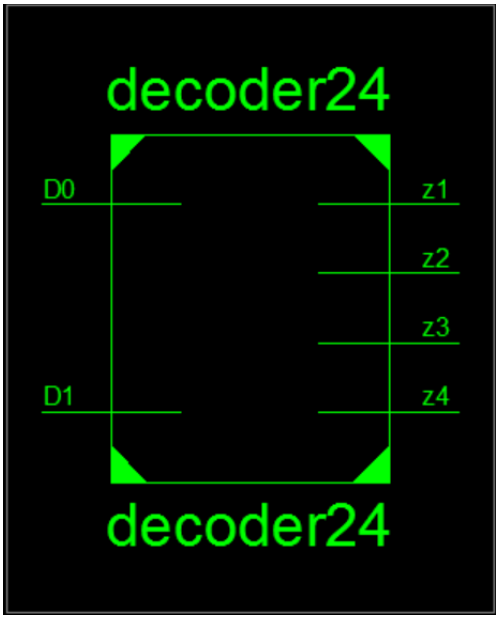

Figure 7: VTS for 2×4 RD

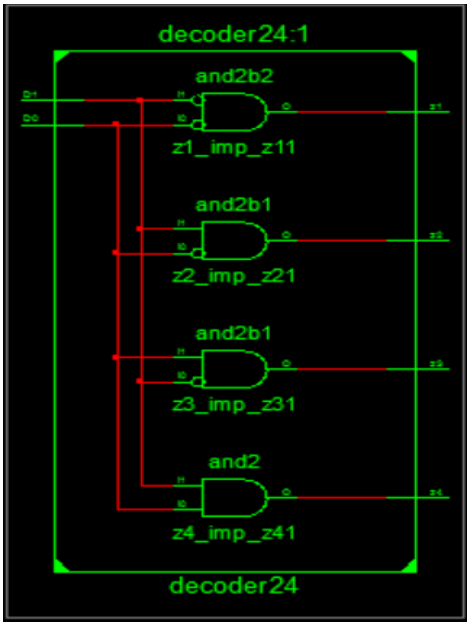

Figure 8: RTL for 2×4 RD

This Fig. 8 shows the RTL Schematic of 2×4 RD. The components of 2×4 RD includes four AND and NOT gate. The RTL Schematic contains all the components inside the view technology.

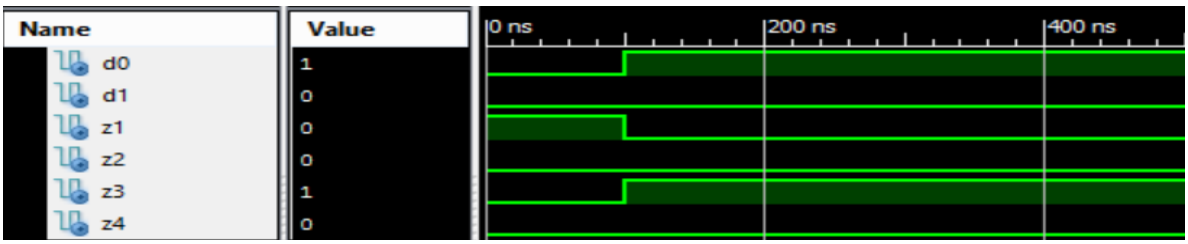

Figure 9: VHDL TB for 2×4 RD

This Fig. 9 shows the TB of 2×4 RD. Here 'I' 'D0' and 'D1' is having the input '10'. When the select input is performed through 2×4 RD, the output comes Z3='1'.

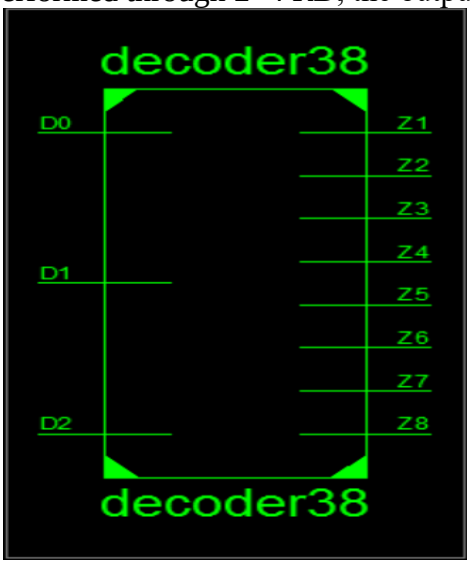

Figure 10: VTS for 3×8 RD

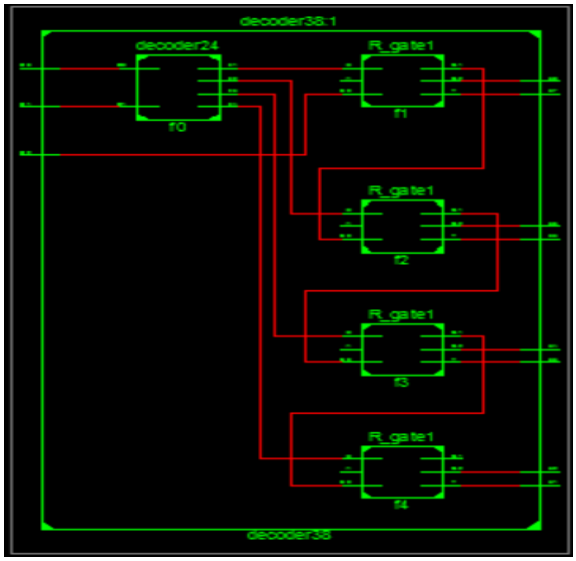

Figure 11: RTL for 3×8 RD

This Fig. 10 shows the VTS of 3×8.RD. Here 'D0', 'D1' and 'D2' is input of 3×8 RD and the output is of maximum four Z1, Z2, Z3, Z4, Z5, Z6, Z7 and Z8. This Fig. 11 shows the RTL Schematic of 3×8

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RD. The components of 3×8 RD include four R gate. The RTL Schematic contains all the components inside the view technology.

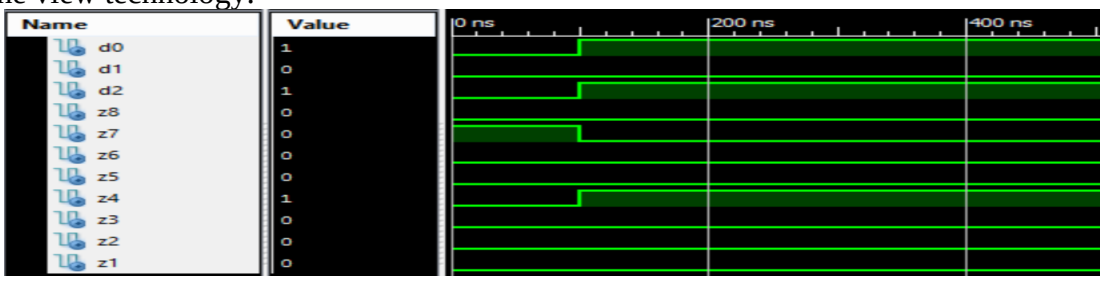

Figure 12: VHDL TB for 3×8 RD

This Fig. 12 shows the TB of 3×8 RD. Here 'D0', 'D1' and 'D2' is having the input '101'. When the select input is performed through 3×8 RD, the output comes Z4='1'.

```
Device utilization summary:
---------------------------

Selected Device : 4vlx80ff1148-12

 Number of Slices:                        2  out of  35840     0%
 Number of 4 input LUTs:                  4  out of  71680     0%
 Number of IOs:                           6
 Number of bonded IOBs:                   6  out of    768     0%

Timing Summary:
---------------
Speed Grade: -12

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 4.868ns
```

(a) 2×4 Decoder

```
Device utilization summary:
---------------------------

Selected Device : 4vlx80ff1148-12

 Number of Slices:                        4  out of  35840     0%
 Number of 4 input LUTs:                  8  out of  71680     0%
 Number of IOs:                          11
 Number of bonded IOBs:                  11  out of    768     1%
 Timing Summary:
 ---------------
 Speed Grade: -12

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 4.999ns
```

(b) 3×8 Decoder

Figure 13: Simulation Result of Decoder

VII. CONCLUSION

In this paper, it has been attempted to comprehensively survey the entire range of current information about Reversible Logic Technology with an emphasis on the application of this technique to make computing systems more efficient. During literature survey, it was found that up-till now very few research papers have been published on design of Arithmetic Logic Unit (ALU) based on reversible logic gates covering very simple and basic functions like AND,OR,X-OR, ADD etc. During literature survey, it has also been found that five most used ALU operations are ADD/SUB, AND, X-OR, OR and NOR. Out of these five most used applications; Addition has more than 80% applications, dominating other ALU operations. Therefore, design of Reversible Logic based 8-bit low-power hybrid adder circuit consisting of carry select and carry ripple adder structures has been implemented. Future development and research work can be carried out for development of the reversible instruction set for the ALU of this research paper.

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