ISSN: 2278-4632
Vol-13, Issue-06, June 2023

Cascading flying capacitor and floating capacitor H-bridges form a seventeen-level inverter

Mr.B.Mahendar[1], Dr.S. Selvakumar Raja[2], Mrs.R.Priyanka[3], Mr.M.Annasrao[4]
[1]Associate Professor, EEE Department, Kakatiya Institute of technology and science for women, Nizamabad, Telangana, India.
[2]Principal & Professor, ECE Department, Kakatiya Institute of Technology and science for Women, Nizamabad, Telangana, India. kitswnzb@gmail.com
[3,4]Assistant Professor, EEE department, Kakatiya Institute of technology and science for women, Nizamabad, Telangana, India.

ABSTRACT

A three-level flying capacitor inverter and cascaded H-bridge modules with float in capacitors have been proposed to generate 17 voltage levels. The current study discusses several features of the suggested inverter, such as capacitor voltage balancing. The simulation results are presented in order to investigate the performance of the suggested converter. The capacitor balancing algorithm's stability has been demonstrated during both transient and steady-state operation. Using one of the pole voltage combinations, all of the capacitors in this circuit can be instantly balanced. Another feature of this design is its ability to generate all voltages from a single dc-link power supply, allowing for back-to-back converter operation. Furthermore, the proposed inverter is capable of operating at all load power factors and modulation indices. Another benefit is that if one of the H-bridges fails, the inverter can still work at full load with a decreased number of levels. The dv/dt and common-mode voltage variations in this setup are quite minimal.

Index Terms—Cascaded H-bridge, flying capacitor, multilevel inverter, 17-level inverter.

I. INTRODUCTION

Since Multilayer inverters have had a profound impact on the efficiency drives operating at medium and high voltages. [1-3]. As seen in [4] and [5], the output voltage approaches a sine wave with a gradually diminishing amount of harmonic content increasing the quantity of voltage levels significantly enhancing the drive's performance. A ground-breaking In the realm of multilayer inverters, a relatively new innovation is represented by the neutral point clamped inverter.6]. Contrarily, [7] discussed the usage of various separate DC sources with H-bridges to stabilize the plasma while producing various voltage levels. The research mentioned in [8] assesses the drawbacks of the a solution to the problem of capacitor imbalance is provided by the cascading multiple rectifier technique. By altering the load current through capacitors, the research given in [9] generates a range of voltages. In this case, selecting redundant states with the same pole voltage allows for the capacitor voltage to be maintained while the capacitor load current is reversed. We combine the thinking of [9] and [7] with that of [10H-bridges in this instance with floating capacitors are employed to generate a range of voltages at the output.. By alternating between redundant states with the same voltage, the capacitor voltages are kept within acceptable ranges. The works discussed in [11–15] give multiple effective control strategies and discuss various elements of using cascaded H-bridges. Common when working with HVDC (high voltage direct current) and also useful for motor driving applications are modular multilevel converters. are another sort of multilevel converter.

[19] Introduces the idea of two types of inverters: one with a neutral point clamp and one with a cascade of flying capacitors. The ABB ACS 2000 is a commercialized version of a similar concept. In [20[Using a flying capacitor inverter with parallel and series capacitors, the concept of increase the level count is discussed. [21] provides an intriguing setup for generating Capacitors were used to generate 17 distinct voltages. However, it takes time to equalize the voltages across the capacitors in [20] and [21]. The fundamental frequency is the only one at which they can cancel each other out. A 17-level inverter design for a single phase is shown in [22]. that makes extensive use of There is a floating load as well as a power supply. This belongs in STATCOM more so. [23] outlines a fascinating technique for running a seventeen-level inverter. In In this research, We describe a new 17-level inverter that uses a single dc source Combining three-level flying

ISSN: 2278-4632
Vol-13, Issue-06, June 2023

capacitor inverters with floating capacitor H-bridges. to get all necessary voltage values. As a result of an experimental validation of the suggested configuration's performance during steady-state and transient operation are given.

II.LITERATURE REVIEW

At the time a number of DC converter arrangements were suggested: buck, boost, SEPIC, buck-boost, and CUK. The lift and buck converter designs allow him to independently raise and drop the resulting voltage, but other converters allow him to play two roles. Many cutting-edge private applications make use of converters for DC to DC with a high voltage gain. A stroke converter is often used to transmit a direct current voltage. The switching pattern of the stroke converter power switch must be big in order to obtain significant voltage gain. As a result, excessive conducted noise is produced, reducing the converter's efficacy. Due to the underlying downtime of the semiconductor switches, a high forced ratio restricts converter replacement frequency. A higher duty cycle also indicates that the diode is more efficient has a lower probability of success. As a result, the diode current transforms into a little pulse with a big immediate magnitude.

"PWM approach for active DC voltage balancing in high-power cascaded multilevel converters" An innovative pulse width modulation (PWM) method for single-phase (or four-wire three-phase) multilevel Cascaded H-Bridge Converters is described by L. Tarisciotti, P. Zanchetta, A. Watson, S. Bifaretti, J. Clare, and P. W. Wheeler.) mode. The suggested method compensates for voltage drops across switching devices and on-state resistances to stabilize Without taking into account the DC-Link voltage reference's amplitude. The converter's waveform quality can be enhanced by using such rectification. This is especially advantageous in low applications requiring high switching frequencies, high power, and low supply voltage. By actively balancing each H-Bridge's DC-Link voltage without any supplementary regulation, and the regulation structure is simplified. loops. To confirm the efficiency of the suggested modulation technique, modelling and comprehensive experimental testing were used.

"Multilevel direct power control—a generic technique for grid-connected multilevel converter applications." Multilevel power converters that are tied into the utility grid J. R. Rodriguez, P. Cortes, each H-Bridge's DC-Link voltage without any supplementary regulation, and the regulation created the generalized multilayer direct power control (ML-DPC) approach. By simply taking into account a small fraction of two-level voltages that are closest to the current switching state, the suggested technique improves on the fundamental DPC operating principle. The power derivatives are required for feedback in the application of this theory, which might cause numerical issues due to being very sensitive to measurement noise when used in experiments. An estimation of the derivative is founded on the synchronous converter-grid architecture. Moreover, an artificial flux monitor being made to help get things in line and make the system more resilient. presence of grid voltage harmonics. Any number of multilevel converter layers can be used with the suggested strategy. The models and experimental data in the course of this research The seven- cascading level H-bridge converters produced as a result are: described.

"Phase-shift modulated capacitor voltage regulation in single-DC-source cascaded H-bridge multilevel converters" K. A. Corzine, H. Sepahvand, J. Liao, M. Ferdowsi, and K. Liao. Another If all If the individual dc voltage sources of the If capacitors were used in place of H-bridge cells, True dc voltage would only be available in a single H-bridge cell. And this will result in an inexpensive adaptor. On the other hand, achieving the required Keeping the voltage of capacitors in check is difficult. An innovative technique for controlling many H-bridge converters in series that share a common dc input is presented in this work. proposed. Utilising phase-shift modulation, it does this. The suggested approach allows for use in H-bridge cells where capacitors have been removed. can be controlled over a wide range of voltages. Experiments and simulations have shown that the suggested method works. to control**.**

III. PROPOSED SYSTEM

The suggested converter uses In a hybrid multilevel topology, three an unsteady capacitor A flying capacitor converter that operates on three levels is cascaded using H-Bridges. Three-phase electrical set-up is depicted in Figure 1. All three variables' values are preserved at Vdc/2: AC1, BC1, and CC1. The capacitors AC2, BC2, and CC2 are maintained at Vdc/4. The capacitors AC3, BC3, and CC3 are held at Vdc/8, whereas the capacitors AC4, BC4, and CC4 are kept at Vdc/16. The intensity made by each H-bridge in a chain can be added to or taken away from the voltage made by the stage before it. Also, the CHBs can be thrown out as well.

By summing the voltages from each stage, the inverter pole voltage is computed. Figure 2 depicts the

ISSN: 2278-4632
Vol-13, Issue-06, June 2023

schematic illustration of the proposed converter's first phase. The switch pairs AS1, AS1, AS2', AS2, AS2', AS3, AS3, AS4, AS4, AS5, AS5, AS6, AS6, AS7, AS7', and AS8' are switched with. the required quantity of dead time in a complementary manner. Each switch combination may be in either the top device (represented by 1) or the bottom device (represented by 0) is turned on) configuration. which are two separate logic states. There are 256 (28) unique switching combinations hence. Pole voltage redundancies, or switching states, is capable of producing an infinite range of voltages. By cycling via arrangements for redundancy switching (for the same pole voltage), it is possible to invert the flow of current through capacitors and adjust the voltage across them.).

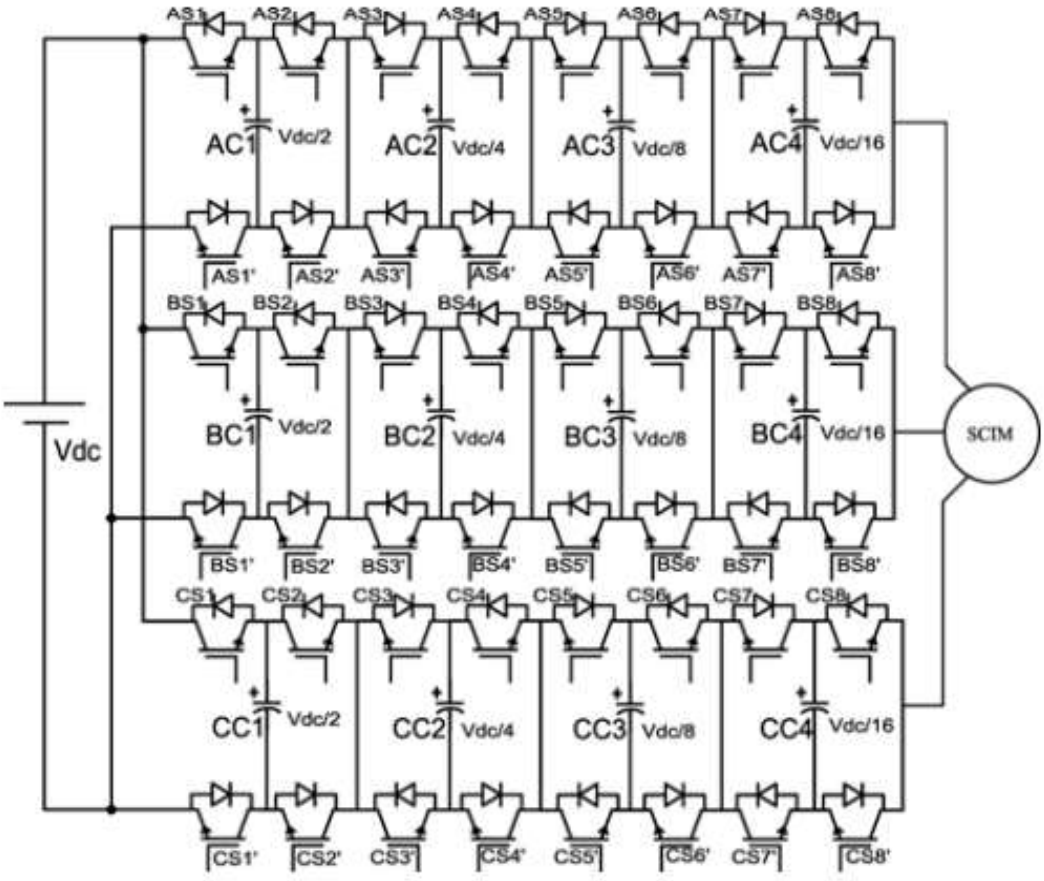


Fig. 1. Three-phase power schematic of the proposed seventeen-level inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a single dc link.

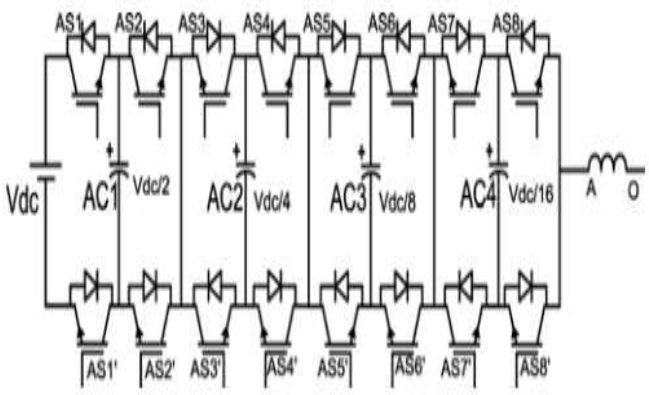


Fig. 2. One phase of the proposed 17-level inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a single dc link.

IV. SPACE VECTOR CONTROL REGION

Pulse-width modulation (PWM) or Pulse-duration modulation (PDM) is a method for reducing the average strength of an electrical signal by breaking the signal up into smaller, discrete chunks. It is necessary to regulate the average load voltage (and load current). by the switch between the supply and the load must be rapidly opened and closed. The total amount of electricity provided to the load rises longer when the switch is on than when it is off. Along with Maximum Power, it is one of the most important approaches. Point Tracking (MPPT) is a method for lowering the output of solar panels to a battery-friendly level. Due to their inertia, inertial loads, such as motors, react slowly, making them less susceptible to harm from PWM's discrete switching. A sufficient

ISSN: 2278-4632
Vol-13, Issue-06, June 2023

PWM switching frequency is required. that the generated waveform has no discernible effect on the load, allowing for the most natural waveform perception possible by the load.

The Depending on the load and the power source, the switching rate (or frequency) might change significantly. intended use. A lamp dimmer, for instance, needs to be toggled numerous times every minute, and so does an electric range. (Utility) frequency of 100 or 120 hertz doubled); switching between a few audio amplifiers switching into the tens or hundreds for a motor drive kilohertz for computer power supplies. PWM's main benefit is that switching devices have almost little power loss at all. When nearly no current flows through a switch while it is off, and nearly no voltage drops across it when it is on. The power loss is small since it is proportional to the voltage times current product. With digital controllers, PWM may be implemented quickly and easily. because of their on/off nature, establish the necessary duty cycle. Pulse-Width Modulation is used in some forms of Furthermore, methods in which the duty cycle is used to send information via a network or telephone line.

Moreover, effective voltage regulators utilize PWM. By transferring voltage to the load while maintaining the right duty cycle, the output will appear to be a voltage at the suitable level. Typically, an inductor and a capacitor are used to filter switching noise.

The output voltage is measured with a single technique. The switch is activated when the voltage falls below the intended level. It prevents the switch from functioning when the output voltage is too high. The three-phase inverter's poles each have the ability to produce one of the following There are 17 different voltage levels that can be applied to the poles, including 0 Vdc/4, Vdc/16, 3 Vdc/8, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, and 15 Vdc/16. The total number of voltage combinations that can be used with the proposed three-phase inverter's pole poles. According to the equation below, a voltage space vector (V SV) is generated for every voltage pole combination.

$$V_{SV} = V_{AN} + V_{BN}\angle 120^{\circ} + V_{CN}\angle 240^{\circ} \qquad (1)$$

Where the three-phase voltages are represented by VAN, VBN, and VC N.

TABLE- I

When the pole sources current, capacitor states and pole voltage redundancy for different switch configurations

S. No.	Pole Voltage	Switch State (S1, S2, S3, S4, S5, S6, S7, S8)	C1ª	C2ª	C3ª	C4ª	S.No	Pole Voltage	Switch State (S1, S2, S3, S4, S5, S6, S7, S8)	C1ª	C2ª	C3ª	C4ª
1	0	(0, 0, 0, 0, 0, 0, 0, 0)	0	0	0	0	42	Vdc/2	(1, 0, 0, 0, 0, 0, 0, 0)	+	0	0	0
2	Vdc/16	(0, 0, 0, 0, 0, 0, 0, 1)	0	0	0	−	43	9 Vdc/16	(0, 1, 0, 0, 0, 0, 0, 1)	−	0	0	−
3		(0, 0, 0, 0, 0, 1, 1, 0)	0	0	−	+	44		(0, 1, 0, 0, 0, 1, 1, 0)	−	0	−	+
4		(0, 0, 0, 1, 1, 0, 1, 0)	0	−	+	+	45		(0, 1, 0, 1, 1, 0, 1, 0)	−	−	+	+
5		(0, 1, 1, 0, 1, 0, 1, 0)	−	+	+	+	46		(1, 0, 0, 0, 0, 0, 0, 1)	+	0	0	−
6		(1, 0, 1, 0, 1, 0, 1, 0)	+	+	+	+	47		(1, 0, 0, 0, 0, 1, 1, 0)	+	0	−	+
7	Vdc/8	(0, 0, 0, 0, 0, 1, 0, 0)	0	0	−	0	48		(1, 0, 0, 1, 1, 0, 1, 0)	+	−	+	+
8		(0, 0, 0, 1, 1, 0, 0, 0)	0	−	+	0	49		(1, 1, 1, 0, 1, 0, 1, 0)	0	+	+	+
9		(0, 1, 1, 0, 1, 0, 0, 0)	−	+	+	0	50	5 Vdc/8	(0, 1, 0, 0, 0, 1, 0, 0)	−	0	−	0
10		(1, 0, 1, 0, 1, 0, 0, 0)	+	+	+	0	51		(0, 1, 0, 1, 1, 0, 0, 0)	−	−	+	0
11	3 Vdc/16	(0, 0, 0, 0, 0, 1, 0, 1)	0	0	−	−	52		(1, 0, 0, 0, 0, 1, 0, 0)	+	0	−	0
12		(0, 0, 0, 1, 0, 0, 1, 0)	0	−	0	+	53		(1, 0, 0, 1,1, 0,0, 0)	+	−	+	0
13		(0, 0, 0, 1, 1, 0, 0, 1)	0	−	+	−	54		(1, 1, 1, 0, 1, 0, 0, 0)	0	+	+	0
14		(0, 1, 1, 0, 0, 0, 1, 0)	−	+	0	+	55	11 Vdc/16	(0, 1, 0, 0, 0, 1,0, 1)	−	0	−	−
15		(0, 1, 1, 0, 1, 0, 0, 1)	−	+	+	−	56		(0, 1, 0, 1, 0, 0, 1, 0)	−	−	0	+
16		(1, 0, 1, 0, 0, 0, 1, 0)	+	+	0	+	57		(0, 1, 0, 1, 1, 0, 0, 1)	−	−	+	−
17		(1, 0, 1, 0, 1, 0, 0, 1)	+	+	+	−	58		(1, 0, 0, 0, 0, 1, 0, 1)	+	0	−	−
18	Vdc/4	(0, 0, 0, 1, 0, 0, 0, 0)	0	−	0	0	59		(1, 0, 0, 1, 0, 0, 1, 0)	+	−	0	+
19		(0, 1, 1, 0, 0, 0, 0, 0)	−	+	0	0	60		(1, 0, 0, 1, 1, 0, 0, 1)	+	−	+	−
20		(1, 0, 1, 0, 0, 0, 0, 0)	+	+	0	0	61		(1, 1, 1, 0, 0, 0, 1, 0)	0	+	0	+
21	5 Vdc/16	(0, 0, 0, 1, 0, 0, 0, 1)	0	−	0	−	62		(1, 1, 1, 0, 1, 0, 0, 1)	0	+	+	−
22		(0, 0, 0, 1, 0, 1, 1, 0)	0	−	−	+	63	3 Vdc/4	(0, 1, 0, 1, 0, 0, 0, 0)	−	−	0	0
23		(0, 1, 0, 0, 1, 0, 1, 0)	−	0	+	+	64		(1, 0, 0, 1, 0, 0, 0, 0)	+	−	0	0
24		(0, 1, 1, 0, 0, 0, 0, 1)	−	+	0	−	65		(1, 1, 1, 0, 0, 0, 0, 0)	0	+	0	0
25		(0, 1, 1, 0, 0, 1, 1, 0)	−	+	−	+	66	13 Vdc/16	(0, 1, 0, 1, 0, 0, 0, 1)	−	−	0	−
26		(1, 0, 0, 0, 1, 0, 1, 0)	+	0	+	+	67		(0, 1, 0, 1, 0, 1, 1, 0)	−	−	−	+
27		(1, 0, 1, 0, 0, 0, 0, 1)	+	+	0	−	68		(1, 0, 0, 1, 0, 0, 0, 1)	+	−	0	−
28		(1, 0, 1, 0, 0, 1, 1, 0)	+	+	−	+	69		(1, 0, 0, 1, 0, 1, 1, 0)	+	−	−	+
29	3 Vdc/8	(0, 0, 0, 1, 0, 1, 0, 0)	0	−	−	0	70		(1, 1, 0, 0, 1, 0, 1, 0)	0	0	+	+
30		(0, 1, 0, 0, 1, 0, 0, 0)	−	0	+	0	71		(1, 1, 1, 0, 0, 0, 0, 1)	0	+	0	−
31		(0, 1, 1, 0, 0, 1, 0, 0)	−	+	−	0	72		(1, 1, 1, 0, 0, 1, 1, 0)	0	+	−	+
32		(1, 0, 0, 0, 1, 0, 0, 0)	+	0	+	0	73	7 Vdc/8	(0, 1, 0, 1, 0, 1, 0, 0)	−	−	−	0
33		(1, 0, 1, 0, 0, 1, 0, 0)	+	+	−	0	74		(1, 0, 0, 1, 0, 1, 0, 0)	+	−	−	0
34	7 Vdc/16	(0, 0, 0, 1, 0, 1, 0, 1)	0	−	−	−	75		(1, 1, 0, 0, 1, 0, 0, 0)	0	0	+	0
35		(0, 1, 0, 0, 0, 0, 1, 0)	−	0	0	+	76		(1, 1, 1, 0, 0, 1, 0, 0)	0	+	−	0
36		(0, 1, 0, 0, 1, 0, 0, 1)	−	0	+	−	77	15 Vdc/16	(0, 1, 0, 1, 0, 1, 0, 1)	−	−	−	−
37		(0, 1, 1, 0, 0, 1, 0, 1)	−	+	−	−	78		(1, 0, 0, 1, 0, 1, 0, 1)	+	−	−	−
38		(1, 0, 0, 0, 0, 0, 1, 0)	+	0	0	+	79		(1, 1, 0, 0, 0, 0, 1, 0)	0	0	0	+
39		(1, 0, 0, 0, 1, 0, 0, 1)	+	0	+	−	80		(1, 1, 0, 0, 1, 0, 0, 1)	0	0	+	−
40		(1, 0, 1, 0, 0, 1, 0, 1)	+	+	−	−	81		(1, 1, 1, 0, 0, 1, 0, 1)	0	+	−	−
41	Vdc/2	(0, 1, 0, 0, 0, 0, 0, 0)	−	0	0	0	82	Vdc	(1, 1, 0, 0, 0, 0, 0, 0)	0	0	0	0

ISSN: 2278-4632
Vol-13, Issue-06, June 2023

When marked on a space vector plane, these 4193 pole voltage combinations are distributed across 817 different space vector points. There may be many Each of the 817 locations of the space vector can have a unique combination of voltages at the poles (voltage protection between phases) and common mode voltages. And furthermore there are a wide variety of redundant switching configurations possible for every pole voltage (redundancy in pole voltage, which can be put to various to provide load balancing). power levels across the phases' worth of capacitors, as was discussed earlier. The 817 points of origin form a hexagonal space vector, which is displayed. schematically in Figure 3. The recommended seventeen-level inverter's space vector control zone is composed of 16 concentric hexagons.

There are no redundant phase voltages in the hexagonal outer space vectors. The second largest hexagon's spots can be made with just two groups of poles voltages and have twofold redundancy. many shared or recurrent voltages. More potential space vector positions can be generated from a wider variety of pole voltages in the smaller inner hexagons. There are sixteen Each space vector location on the innermost hexagon has two pole voltage options, each with a different common mode voltage. Consequently, the seventeen pole voltage combinations that make up the zero state at the centre all result in zero differential mode voltage.

This approach has been found to quickly balance the capacitor voltages for 17-pole voltage levels across power factor and load current variations. Zero volts, sixteen volts, eight volts, three volts, four volts, five volts, eight volts, two volts, nine volts, eleven volts, fifteen volts, seven volts, and sixteen volts. However, utilising the suggested design, 31 different pole voltage levels can be produced by cycling through all possible combinations of pole voltage switching. Capacitor voltages can only be balanced in a fundamental cycle throughout the remaining fourteen levels. The 17 pole voltage levels listed above, for which It is feasible to balance the voltage on a capacitor instantly. can be generated by one of 82 possible switching combinations (see Table I). Table I demonstrates the effects of 82 switching topologies on the For positive current flow, or when As seen in Figure 3, the pole represents the electrical current's origin. state (charge or discharge) of each capacitor.2. The opposite-direction current. For instance, there are a number of redundant switching combinations to choose from in order to produce the Vdc/16 pole voltage that the controller requires. The capacitors' state of charge is affected in a different way by each switching configuration. When the switching state is applied [see Fig. 3] when the When the switching state is (1, 1, 1, 1, 1) (see Table I), the capacitor C4 discharges while the pole is delivering current.) is used. to transmit the balance of the C4 capacitors to one of the other four The desired voltage (Vdc/16) is then restored using switching combinations as shown in Figure 3. When applying the capacitor C4 current during the 0 0 0 0 0 0 0 1 0 switching state grows.ed. flows in the opposite direction and charges. Nevertheless, the capacitor C3 discharges during this operation. If charging capacitor C3, we employ a redundant switching state sequence of (0, 0, 0, 1, 1, 1, 1, 0, 1, 0) to discharge capacitor C2 [see Fig. 3.]. Figure 3 depicts one of several redundant switching configurations. As shown in Figure 3., capacitor C1 discharges when a state is changed It is applied (0, 1, 1, 0, 1, 0, 1, 0). The remaining capacitors have been charged. And lastly According to Fig. 3, All When a current is present in a positive direction, four capacitors are charged. when the state of switching (1, 0, 1, 0, 1, 0, 1, 0) is applied. By repeatedly cycling through the same voltage combinations at each pole it is possible to keep all capacitor voltages at their required levels while making the positive current flow at a pole voltage of Vdc/16. If it is necessary to deplete all of the capacitors, then capacitor C4 will be depleted first. During successive switching cycles, the remaining capacitors may be depleted in preparation for charging the capacitor C4 in the event that it is necessary. The consequence of capacitor voltages is opposite for current flowing in the wrong direction.

Fig. 4 depicts the full stated capacitor voltage equalization using a 16-volt DC supply per pole. Here, the capacitor voltage variation for Vdc/16 pole voltage has been demonstrated for current flowing in the positive direction. In the case of Different voltages for each pole: Vdc/8, 3 Vdc/16, Vdc/4, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2, 9 Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16. Using a comparable method, we can equalize the voltages of all the capacitors, including and Vdc. Any CHB module's switching frequency is limited by the PWM toggling of the converter. frequency. This is because the switching state is applied in synchrony with each PWM transition and is latched until the subsequent

ISSN: 2278-4632
Vol-13, Issue-06, June 2023

PWM transition. Additionally, output pole voltage supporting capacitors alone. swapped in this system.

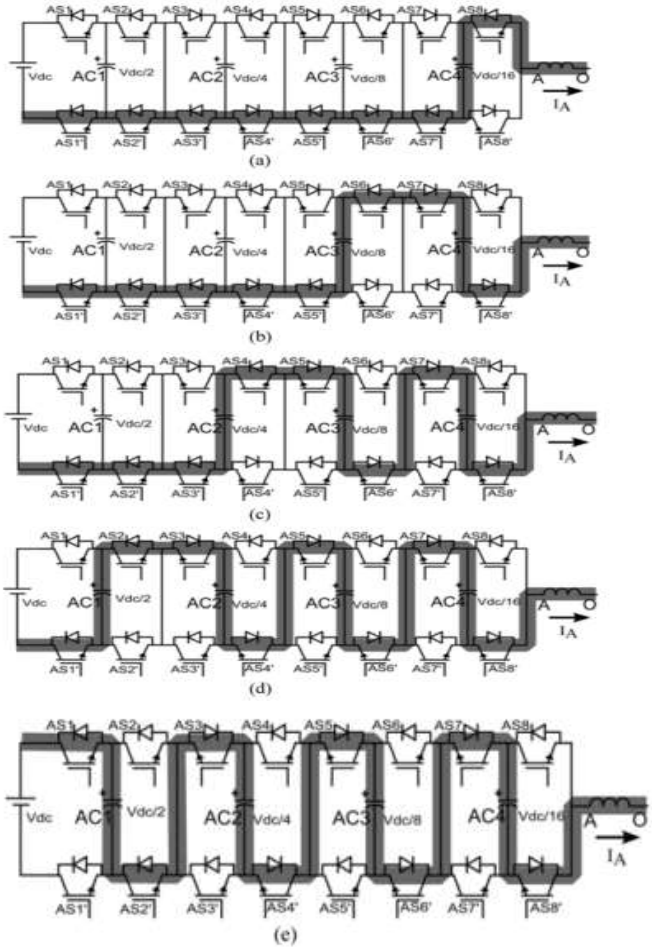


Fig. 3. Switching Redundancies for Vdc/16 Pole.

Voltage Current path for changing states is shown in (a) (0, 0, 0, 0, 0, 0, 0, 1). (0, 0, 0, 0, 0, 1, 0) (b) The current state-changing procedure. (c) The present means of making a transition from one state to another (0, 0, 0, 1, 1, 0, 1, 0). (d) The current route taken when transitioning between states (0, 1, 1, 0, 1, 0, 1, 0). (1, 0, 1, 0, 1, 0, 1, 0) is the current path for switching states.

The change state is determined by the needed level, capacitor voltage condition, and current. generator generates the proper switching state. after receiving the instantaneous level data. This is accomplished by using an FPGA look-up table to construct the circuitry shown in Table I. This switching state is supplied into a circuit that generates adequate dead time and creates the complimentary operation of the top and bottom devices, as evidenced by their gating signals. The dead time generation circuit is included within the FPGA as well, thus no additional components are required to maintain a consistent dead band.

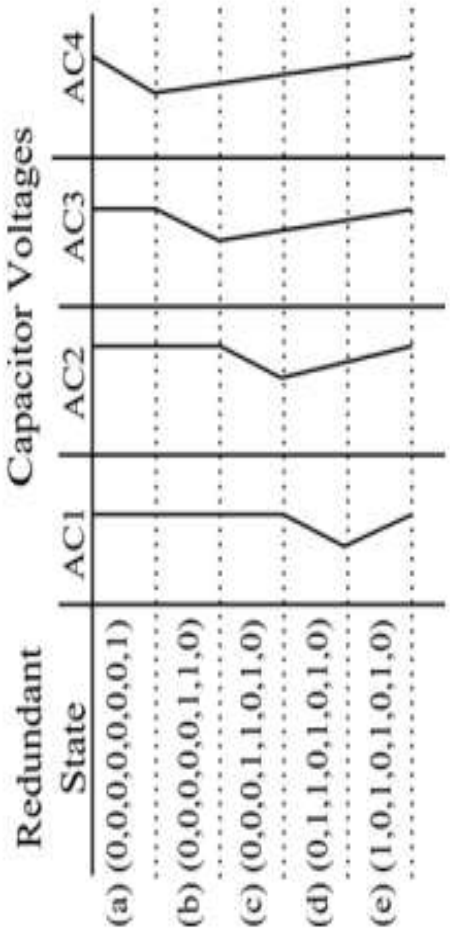


Fig. 4 .Capacitor voltage variation with application of redundant states for pole voltage of Vdc/16 for positive current

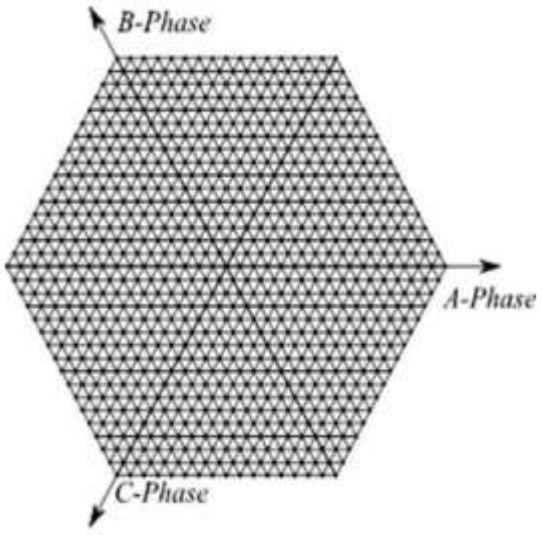


Fig. 5. Space vector polygon formed with the proposed five-level inverter

V. RESULTS AND DISCUSSION

Fig. 6 displays the simulation Schematic depicting the controller that will make the signs that tell the inverter when to switch. The control algorithm, such as It's possible that a specific range of voltage

ISSN: 2278-4632
Vol-13, Issue-06, June 2023

reference values is needed for a V/f, Vector control, or other method. each of the three phases. Using a level-shifted carrier to make a space vector PWM signal technique with these voltage levels.

Model for simulation

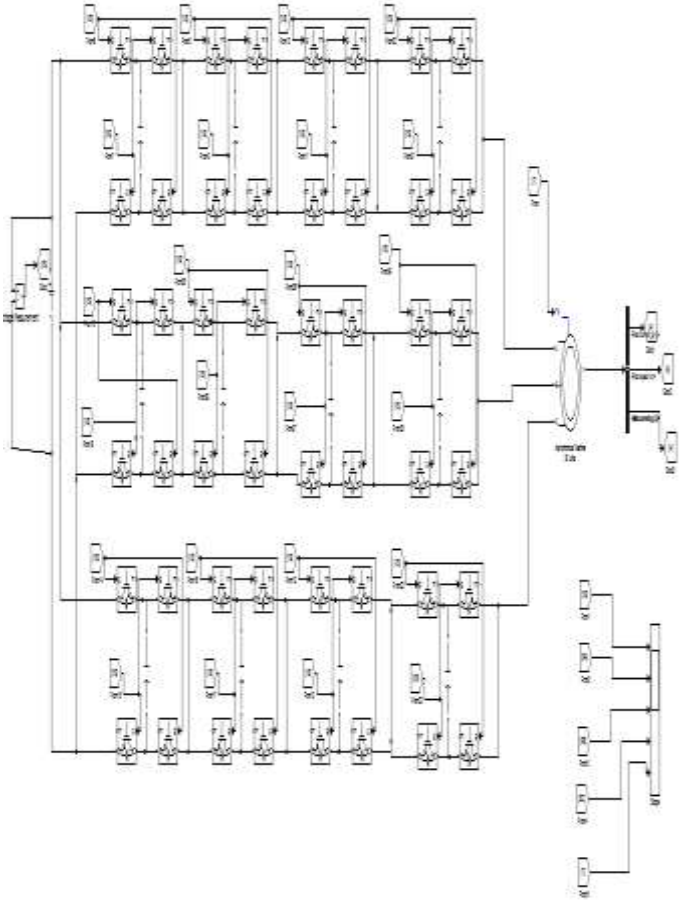


Fig. 6. Simulation model

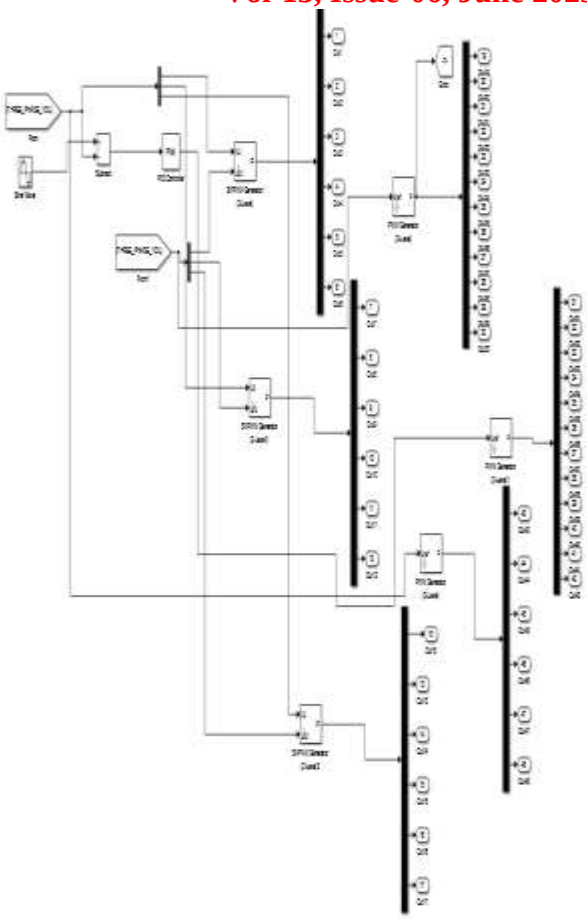


Fig. 7. SVPWM Control diagram

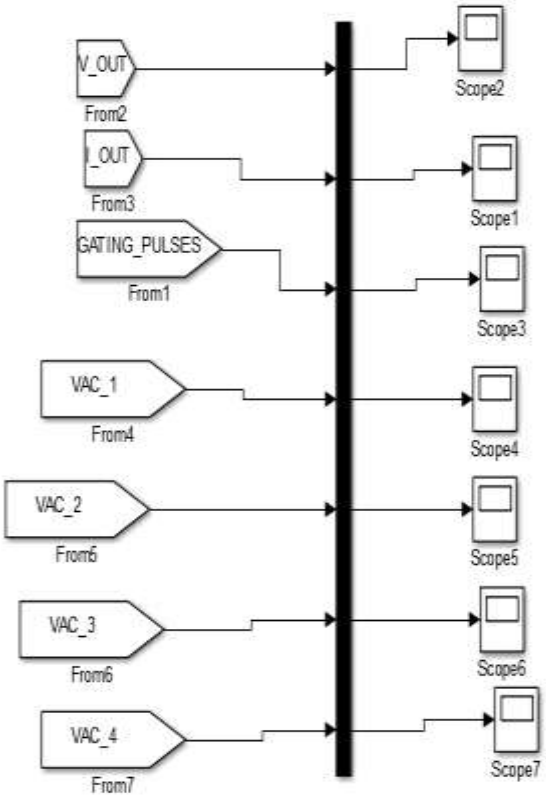


Fig. 8 .Results

ISSN: 2278-4632
Vol-13, Issue-06, June 2023

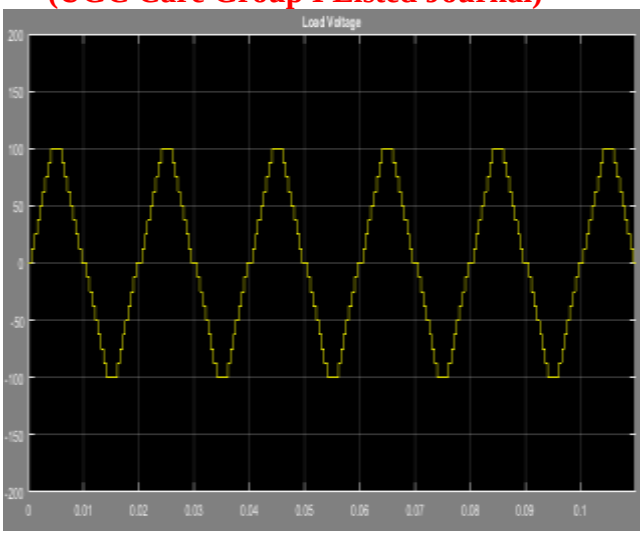


Fig. 9. Output voltage

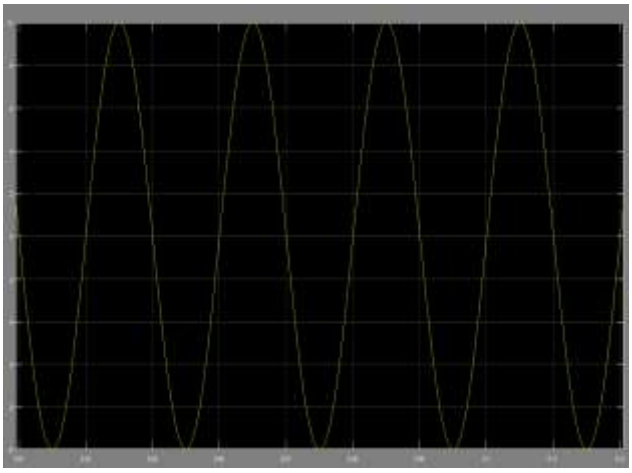
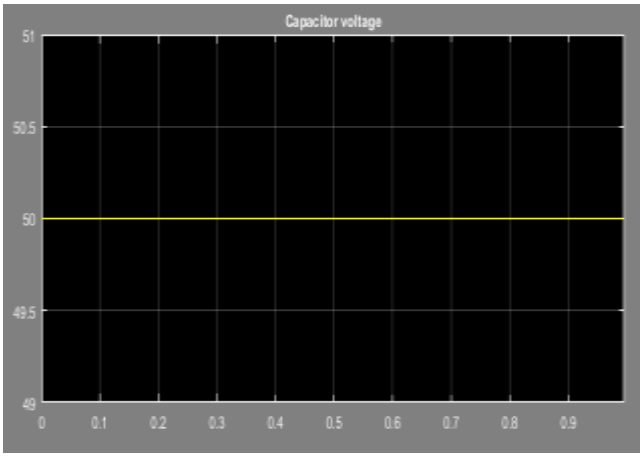
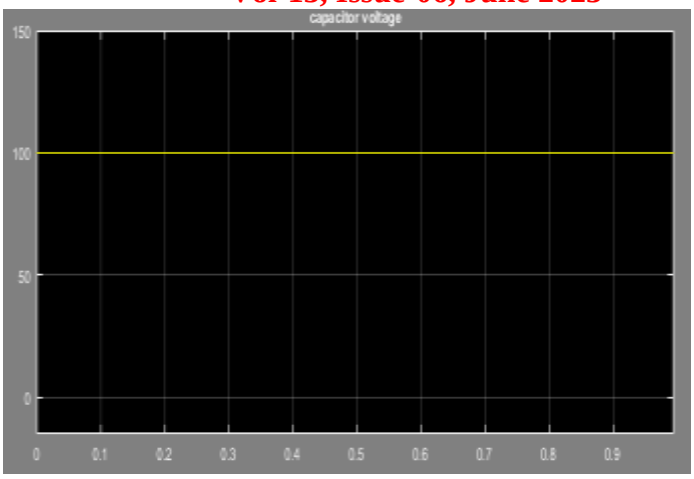


Fig. 10 .Output current

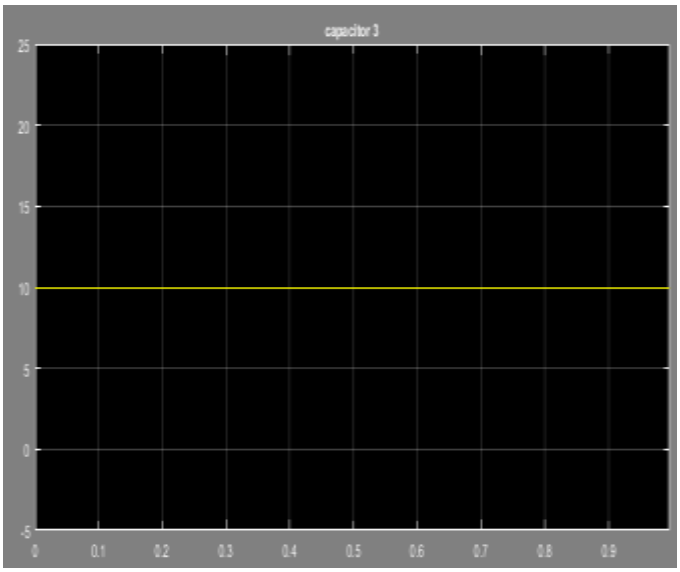
Fig. 8 displays the motor voltages (including those of capacitors, phases, and and motor pole voltages. It is evident that the output voltage steps are quite small and There is no change in the power of the capacitors. 0.40 at 20 Hertz, 0.60 at 30 Hertz, and 0.80 at 40 Hertz. for the modulation index. are also used to run the motor (see Figs. 11).



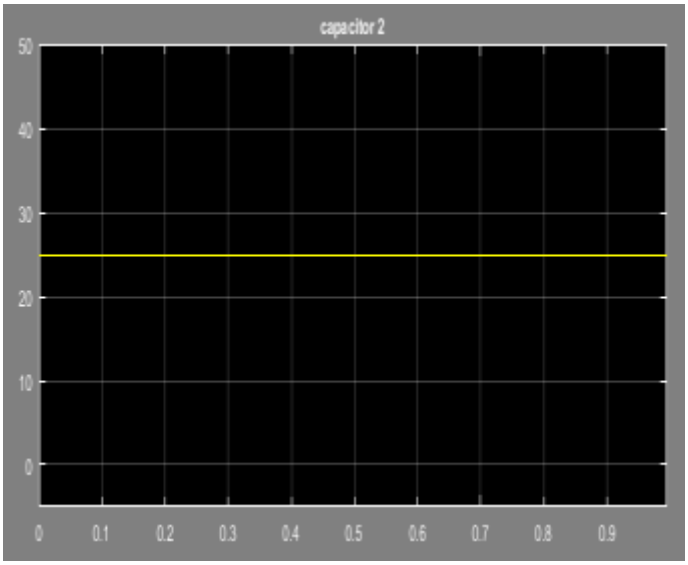
(a)



(b)



(c)



(d)

Fig. 11. Capacitor voltages

VI. CONCLUSION

A new 17-level inverter configuration formed by cascading a three-level flying capacitor and three floating capacitor H-bridges has been proposed for the first time. The voltages of each of the capacitors are

ISSN: 2278-4632
Vol-13, Issue-06, June 2023

controlled instantaneously in few switching cycles at all loads and power factors obtaining high performance output voltages and currents. The proposed configuration uses a single dc link and derives the other voltage levels from it. This enables back-to-back converter operation where power can be drawn and supplied to the grid at prescribed power factor. Also, the proposed 17-level inverter has improved reliability. In case of failure of one of the H-bridges, the inverter can still be operated with reduced number of levels supplying full power to the load. This feature enables it to be used in critical applications like marine propulsion and traction where reliability is of highest concern. Another advantage of the proposed configuration is modularity and symmetry in structure which enables the inverter to be extended to more number of phases like e-phase and six-phase configuration with the same control scheme. The proposed inverter is analyzed and its performance is experimentally verified for various modulation indices and load currents by running a three-phase 3-kW squirrel cage induction motor.

REFERENCES

[1] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Appl., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[2] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," IEEE Ind. Electron. Mag., vol. 2, no. 2, pp. 28–39, Jun. 2008.

[3] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B.Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[4] A. M. Massoud, S. Ahmed, P. N. Enjeti, and B. W. Williams, "Evaluation of a multilevel cascaded-type dynamic voltage restorer employing discontinuous space vector modulation," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2398–2410, Jul. 2010.

[5] S. Rivera, S. Kouro, B. Wu, S. Alepuz, M. Malinowski, P. Cortes, and J. R. Rodriguez, "Multilevel direct power control—a generalized approach for grid-tied multilevel converter applications," IEEE Trans. Power Electron., vol. 29, no. 10, pp. 5592–5604, Oct. 2014.

[6] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[7] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A non-conventional power converter for plasma stabilization," in Proc. IEEE 19th Annu. Power Electron. Spec. Conf. Rec., Apr. 11–14, 1988, vol. 1, pp. 122–129.

[8] L. Sun, W. Zhenxing, M. Weiming, F. Xiao, X. Cai, and L. Zhou, "Analysis of the DC-Link capacitor current of power cells in cascaded H-bridge inverters for high-voltage drives," IEEE Trans. Power Electron., to be published.

[9] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in Proc. IEEE 23rd Annu. Power Electron. Spec. Conf., Jun. 29–Jul. 3, 1992, vol. 1, pp. 397–403.

[10] Z. Du, L. M. Tolbert, J. N. Chiasson, B. Ozpineci, H. Li, and A. Q. Huang, "Hybrid cascaded H-bridges multilevel motor drive control for electric vehicles," in Proc. IEEE 37th Power Electron. Spec. Conf., Jun. 18–22, 2006, pp. 1–6.

[11] G. Adam, I. Abdelsalam, K. Ahmed, and B. Williams, "Hybrid multilevel converter with cascaded h-bridge cells for HVDC applications: Operating principle and scalability," IEEE Trans. Pow. Electron., to be published.

[12] H. Sepahvand, J. Liao, and M. Ferdowsi, "Investigation on capacitor voltage regulation in cascaded H-bridge multilevel converters with fundamental frequency switching," IEEE Trans. Ind. Electron., vol. 58, no. 11, pp. 5102–5111, Nov. 2011.

[13] J. Liu, K. W. E. Cheng, and Y. Ye, "A cascaded multilevel inverter based on switched-capacitor for high-frequency AC power distribution system," IEEE Trans. Power Electron., vol. 29, no. 8, pp. 4219–4230, Aug. 2014.

[14] L. Tarisciotti, P. Zanchetta, A. Watson, S. Bifaretti, J. Clare, and P. W. Wheeler, "Active DC voltage balancing PWM technique for highpower cascaded multilevel converters," IEEE Trans. Ind. Electron., vol. 61, no. 11, pp. 6157–6167, Nov. 2014.

[15] H. Sepahvand, J. Liao, M. Ferdowsi, and K. A Corzine, "Capacitor voltage regulation in single-DC-source cascaded H-bridge multilevel converters using phase-shift

ISSN: 2278-4632
Vol-13, Issue-06, June 2023

modulation," IEEE Trans. Ind. Electron., vol. 60, no. 9, pp. 3619–3626, Sep. 2013.

[16] Z. Zheng, K. Wang, Lie Xu, and Y. Li, "A hybrid cascaded multilevel converter for battery energy management applied in electric vehicles," IEEE Trans. Power Electron., vol. 29, no. 7, pp. 3537–3546, Jul. 2014.

[17] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," IEEE Trans. Power Electron., vol. 25, no. 7, pp. 1786–1799, Jul. 2010.

[18] B. Riar and U. Madawala, "Decoupled control of modular multilevel converters using voltage correcting modules," IEEE Trans. Pow. Electron., to be published.

[19] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, M. Winkelnkemper, and N. Celanovic, "Active neutral-point-clamped multilevel converters," in Proc. IEEE 36th Power Electron. Spec. Conf., Jun. 16, 2005, pp. 2296– 230.

[20] T. Chaudhari, A. Rufer, and P. K. Steimer, "The common cross connected stage for the 5 L ANPC medium voltage multilevel inverter," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2279–2286, Aug. 2010.

[21] M. Glinka, "Prototype of multiphase modular-multilevel-converter with 2 MW power rating and 17-level-output-voltage," in Proc. Power Electron. Spec. Conf., 2004, vol. 4, pp. 2572–2576.

[22] G. Baoming and F. Z. Peng, "Speed sensor less vector control induction motor drives fed by cascaded neutral point clamped inverter," in Proc. Appl. Power Electron. Conf. Expo., Feb. 15–19, 2009, pp. 1991–1997.

[23] G. Baoming, F. Z. Peng, "An effective SPWM control technique for 1 MVA 6000 V cascaded neutral point clamped inverter," in Proc. IEEE Ind. Appl. Soc. Annu. Meeting, Oct. 5–9, 2008, pp. 1–6.

[24] R. S. Kanchan, M. R. Baiju, K. K. Mohapatra, P. P. Ouseph, and K. Gopakumar, "Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages," in Proc. IEEE Elect. Power Appl., vol. 152, no. 2, pp. 3297–309, Apr. 2005